ASiC / ASSP
CUSTOMER INFORMATION #10

Whisker growth in RoHS-compliant packages

The growth of whiskers on tin-plated surfaces is a phenomenon engineers are familiar with and one which can pose a risk to electronics units if, for example, neighboring pins short circuit. It is believed that these crystalline tin deposits, which 'grow' spontaneously from the tin surface, are caused by mechanical stresses which occur when intermetallic copper-tin (CuSn) phases form in the grain boundaries; to date, however no one has really completely understood or provided a full explanation for this mechanism.

For decades the use of leaded tin alloys for solder and solderable surfaces throughout the world proved successful in prohibiting the formation of whiskers. The lead ban for electronics, as stipulated by the EU's RoHS (Restriction on the Use of Certain Hazardous Substances) directive, has, however, now raised a subject long considered unproblematic.

Preventing the growth of whiskers in iC-Haus products

COB on nickel-gold surfaces
Although the growth of whiskers is not restricted to tin and its alloys, the use of 'non-tin' surfaces is a suitable method of evading this growth. In its products based on COB technology (BMST, BLCC etc.) iC-Haus uses nickel-gold (NiAu) surfaces to prevent whiskers forming.

BGA
In the lead-free version of the BGA solder depots with tin-silver-copper (SnAgCu) solder are used. As with lead the silver and copper components reduce the creation of whiskers.

Standard plastic packages with matte tin surfaces
In its standard plastic package products (such as SOIC, SOT, MQFP, PLCC, TSSOP and QFN, for example) iC-Haus and its assembly subcontractors are going with the world trend and adopting pure tin as the best replacement for the tin-lead alloys previously used. The following measures are being adhered to in an attempt to prevent the growth of whiskers (cf. Joint Publication 002 (JP002), *Current Whisker Theory and Mitigation Practices Guideline*, published by JEDEC and IPC, 1st edition, March 2006):

- Structure: matte tin
- Layer thickness: min. 10 µm
- Annealing layer: post plate bake at 150 °C/1 hour
- CTE matching: leadframe with a suitable coefficient of expansion (> 15 ppm/K)

The contacts in QFN packages, all of which are on the underside of the device, are completely wet with solder during reflow soldering.

The effectiveness of these measures is being comprehensively monitored according to the recommendations of JESD22A121.01 and NEMI.

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