iC-GFP

IO-Link SLAVE TRANSCEIVER

preliminary

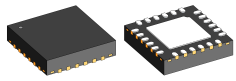
FEATURES

- IO-Link COM3-compliant slave transceiver (230.4 kBaud)
- Dual-channel switches, configurable for high-side, low-side and push-pull operation with tristate function
- Configuration via SPI interface with secured data transmission
- Switches are programmable current limited
- Switches, iC supply and feedback channel are protected against reverse polarity
- Output current of up to 200 mA per channel
- Parallel connection of both channels possible
- The channels can be inverted for antivalent output
- Sensor communication request function (*IO-Link wake-up*)
- Wide supply voltage range of 4.5 to 36 V
- Sensor parametrization via two feedback channels (up to 36 V)
- Switching converter and linear regulators with 5/3.3/2.5/1.8 V output voltage
- On-chip digital temperature sensor with alarm
- IRQ output with excess temperature, overload and under-voltage
- Driver shut-down on errors

APPLICATIONS

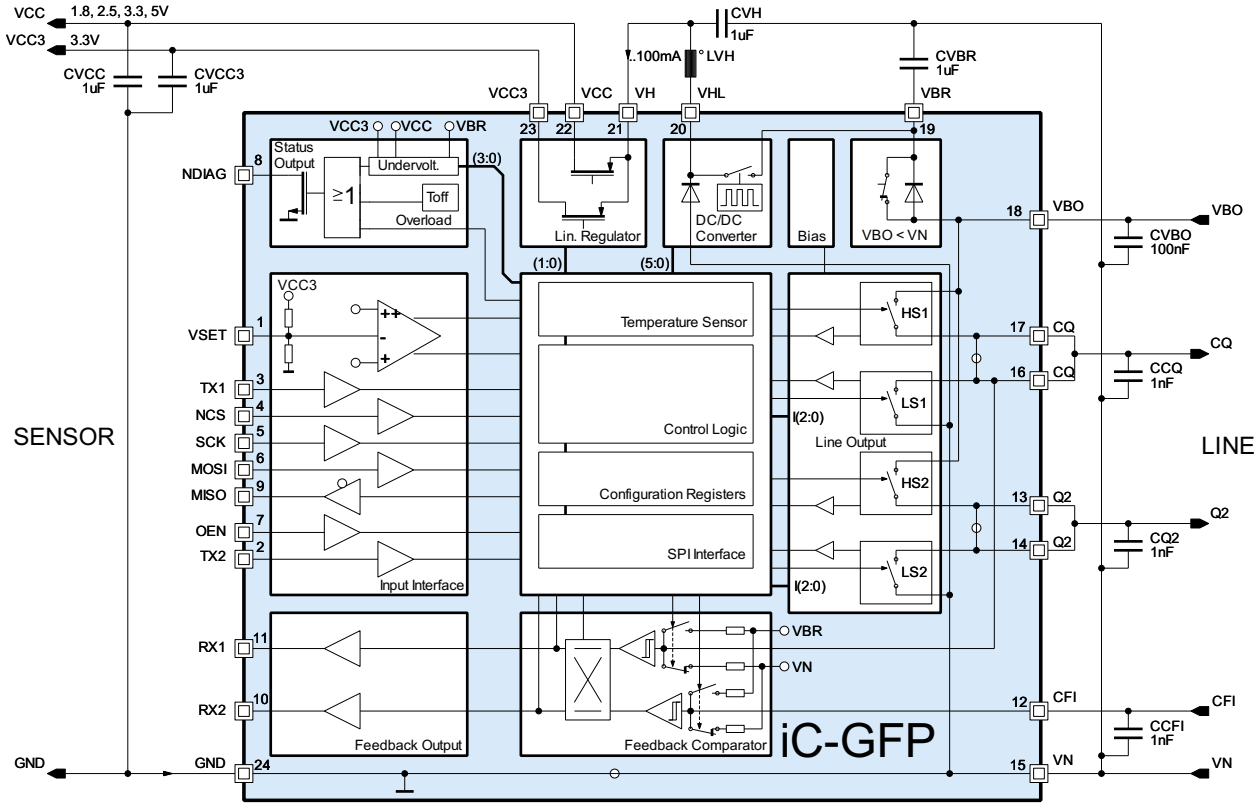
- IO-Link slaves
- I/O sensor interface
- Digital sensors
- Proximity switches
- Light barriers

PACKAGES



QFN24 4 mm x 4 mm
(RoHS compliant)

BLOCK DIAGRAM



DESCRIPTION

iC-GFP is a fully IO-Link COM3-compliant transceiver iC with two independent switching channels which enables digital sensors to drive peripheral elements, such as programmable logic controllers (PLC) and relays, for example.

The outputs can be configured for push-pull, high-side or low-side operation. A synchronized mode permits both channels to work as one or in antivalent mode. The switches are designed to cope with high driver currents of up to 200 mA, are current limited, and also short-circuit-proof in that they shut down with excessive temperature or overload. The output current limit is set digitally via SPI.

The overload protection is accomplished in a way so that capacitive loads can be switched with low repeat rates without the protective circuitry cutting in. In the event of excess temperature an error message is generated immediately.

The iC-GFP performs a self-diagnostic function and signals errors at the open-collector output, NDIAG. The outputs are shut down in case of errors.

To avoid error signalling during power-up, the outputs remain at high impedance for ca. 50 ms.

The chip acts as an SPI slave and allows function configuration via secured register access. It also features diagnostic registers and supports *communication requests* (= IO-Link *wake-up*) at pin CFI or CQ which generate interrupt signals at pin NDIAG.

The pins on the 24 V line side of the sensor interface (VBO, CQ, Q2, VN, and CFI) are protected against reverse polarity. This makes any external reverse polarity protection diodes superfluous.

iC-GFP features an integrated switching converter which generates voltages VCC (5, 3.3, 2.5, 1.8 V, selectable) and VCC3 (3.3 V) with the aid of two downstream linear regulators. For *medium* currents the inductor may as well be replaced by a resistor (e.g. 170 Ω), resulting though in a considerably less efficiency. If only a low current is required inductor LVH may be omitted completely; the linear regulators are then powered directly by VBR.

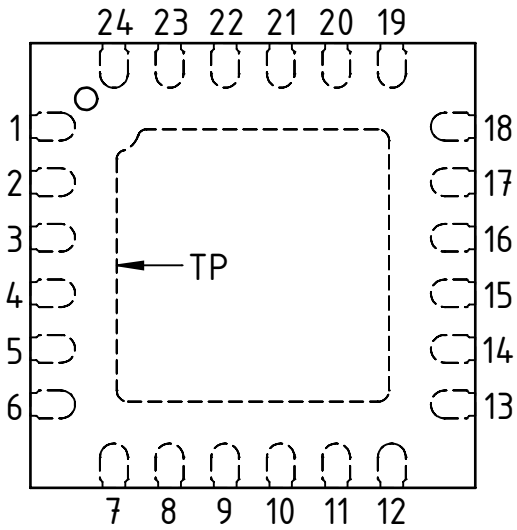
The switching regulator comes equipped with a spread-spectrum oscillator to reduce interferences.

The connected sensor can be parametrised using the feedback channels (CFI/CQ → RX1/RX2).

A digital temperature sensor provides the chip temperature, readable by the MCU. A programmable temperature alarm is provided as well.

PACKAGING INFORMATION

PIN CONFIGURATION QFN24 4 mm x 4 mm



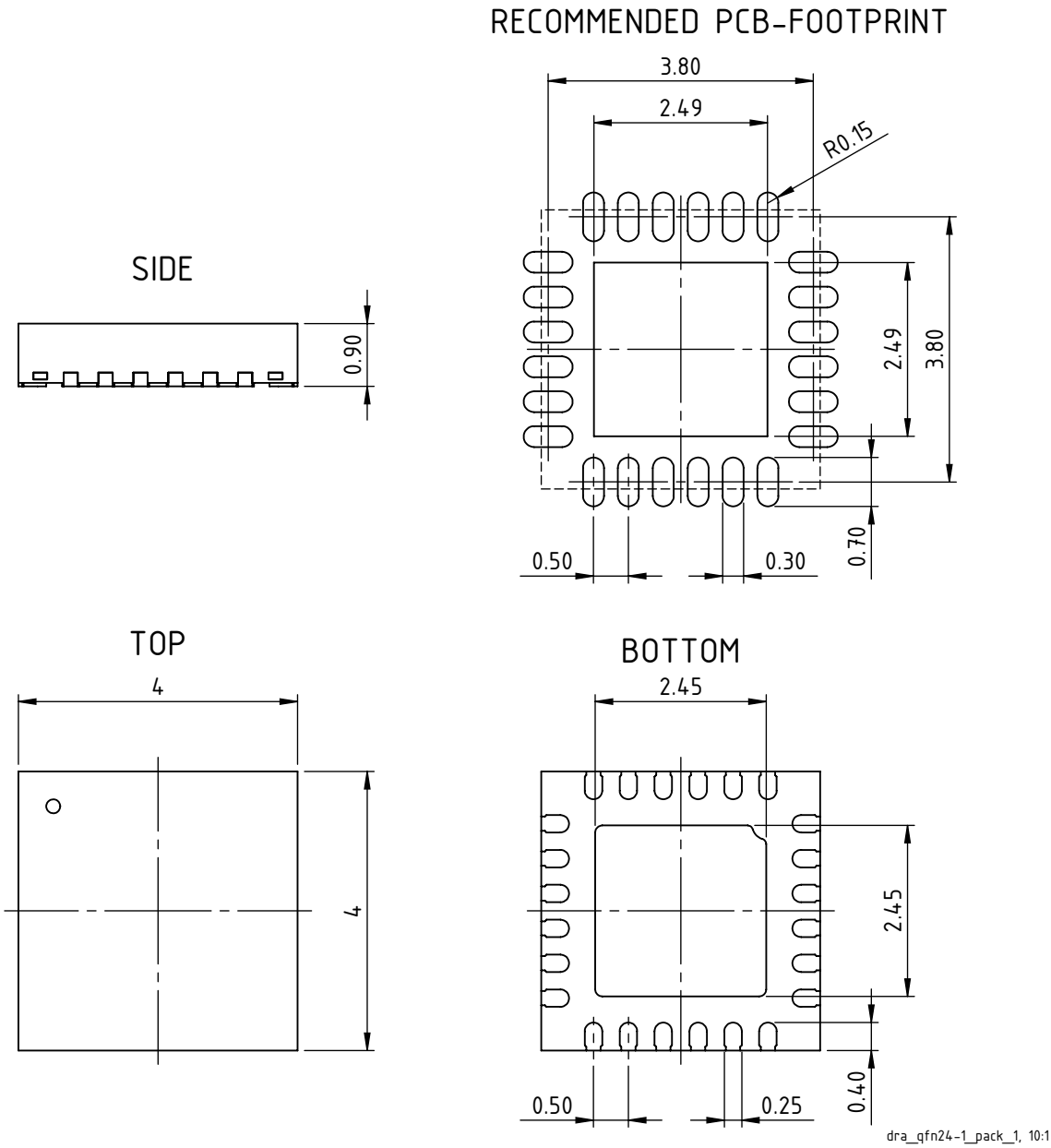
PIN FUNCTIONS

No.	Name	Function
1	VSET	Voltage Configuration for VCC
2	TX2	Input Channel 2
3	TX1	Input Channel 1
4	NCS	Chip Select
5	SCK	SPI Serial Clock
6	MOSI	Master Output Slave Input
7	OEN	Output Enable Input
8	NDIAG	Diagnostics Output
9	MISO	Master Input Slave Output
10	RX1	Feedback Output 1
11	RX2	Feedback Output 2
12	CFI	Feedback Channel Input
13	Q2	Output Channel 2
14	Q2	Output Channel 2
15	VN	Ground
16	CQ	I/O Channel
17	CQ	I/O Channel
18	VBO	Power Supply
19	VBR	Power Supply for switching converter
20	VHL	Switching Converter Inductance
21	VH	Input Linear Regulators
22	VCC	5/3.3/2.5/1.8 V Sensor Supply
23	VCC3	3.3 V Sensor Supply
24	GND	Sensor Ground
	TP	Thermal Pad

The *Thermal Pad* is to be connected to a Ground Plane (VN) on the PCB.
Only pin 1 marking on top or bottom defines the package orientation (iC-GFP label and coding is subject to change).

PACKAGE DIMENSIONS QFN24 4 mm x 4 mm

All dimensions given in mm.



ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed. Absolute Maximum Ratings are no operating conditions! Integrated circuits with system interfaces, e.g. via cable accessible pins (I/O pins, line drivers) are per principle endangered by injected interferences, which may compromise the function or durability. The robustness of the devices has to be verified by the user during system development with regards to applying standards and ensured where necessary by additional protective circuitry. By the manufacturer suggested protective circuitry is for information only and given without responsibility and has to be verified within the actual system with respect to actual interferences.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VBO	Power Supply at VBO	Referenced to lowest voltage of VN, VBR, CQ, Q2, CFI, VH, VHL		36	V
			Referenced to highest voltage of VN, VBR, CQ, Q2, CFI, VH, VHL	-36		V
G002	I(VBO)	Current in VBO		-10	600	mA
G003	VBR	Voltage at VBR	Referenced to lowest voltage of VN, VBO, CQ, Q2, CFI, VH, VHL		36	V
			Referenced to highest voltage of VN, VBO, CQ, Q2, CFI, VH, VHL	-36		V
G004	I(VBR)	Current in VBR		-600	150	mA
G005	V(VH)	Voltage at VH	Referenced to lowest voltage of VN, VBR, VBO, CQ, Q2, CFI, VHL		36	V
			Referenced to highest voltage of VN, VBR, VBO, CQ, Q2, CFI, VHL	-36		V
G006	I(VH)	Current in VH		-5	120	mA
G007	V(VHL)	Voltage at VHL	Referenced to lowest voltage of VN, VBR, VBO, CQ, Q2, CFI, VH		36	V
			Referenced to highest voltage of VN, VBR, VBO, CQ, Q2, CFI, VH	-36		V
G008	I(VHL)	Current in VHL		-150	5	mA
G009	V(VN)	Voltage at VN vs. GND		-0.5	0.5	V
G010	I(VN)	Current in VN	VN < VBO	-500	500	mA
			VN > VBO	-10	10	mA
G011	V()	Voltage at VCC, VCC3		-0.3	7	V
G012	I()	Current in VCC, VCC3		-50	10	mA
G013	V()	Voltage at CQ, Q2	Referenced to lowest voltage of VN, VBO, VBR, CQ, Q2, CFI, VH, VHL		36	V
			Referenced to highest voltage of VN, VBO, VBR, CQ, Q2, CFI, VH, VHL	-36		V
G014	I()	Current in CQ, Q2		-400	400	mA
G015	V(CFI)	Voltage at CFI	Referenced to lowest voltage of VN, VBO, VBR, CQ, Q2, VH, VHL		36	V
			Referenced to highest voltage of VN, VBO, VBR, CQ, Q2, VH, VHL	-36		V
G016	I(CFI)	Current in CFI		-4	4	mA
G017	V()	Voltage at MOSI, SCK, NCS, TX1, TX2, VSET, OEN, RX1, RX2, NDIAG, MISO		-0.3	7	V
G018	I()	Current in MOSI, SCK, NCS, TX1, TX2, VSET, OEN		-4	4	mA
G019	I()	Current in RX1, RX2, MISO		-70	70	mA
G020	I()	Current in NDIAG		-4	70	mA
G021	Vd()	ESD Susceptibility at all pins	HBM, 100 pF discharged through 1.5 kΩ		2	kV
G022	Tj	Junction Temperature		-40	150	°C
G023	Ts	Storage Temperature Range		-40	150	°C

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

THERMAL DATA

Operating Conditions: VBO = 4.5...36 V (referenced to VN), Tj = -40...125 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range (extended range on request)		-40		85	°C
T02	Rthja	Thermal Resistance Chip/Ambient	Surface mounted, thermal pad soldered to ca. 2 cm² heat sink		30	40	K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VBO = 4.5...36 V (referenced to VN), Tj = -40...125 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VBO	Permissible Supply Voltage	Referenced to VN	4.5	24	36	V
002	I(VBO)	Supply Current in VBO	No load, VH conected to VBR, I(CQ) = I(Q2) = 0, CQ/Q2 switched on			5.5	mA
003	Vs(VBR)	Saturation Voltage at VBR	Vs(VBR) = V(VBO) − V(VBR); I(VBR) = -20 mA I(VBR) = -50 mA			 1 1.2	 V V
004	VH	Permissible Voltage at VH		5		36	V
005	I(VH)	Supply Current in VH	VH = 8 V, no load, I(VCC) = I(VCC3) = 0, V(OEN) = hi	0.5		3	mA
006	Vc()hi	Clamp Voltage hi at VBO, VBR vs. VN	I() = 10 mA	36			V
007	Vc()lo	Clamp Voltage lo at VBO, VBR vs. VN	I() = -10 mA			-36	V
008	Vc()hi	Clamp Voltage hi at CQ, Q2 vs. VN	I() = 1 mA, VBO > VN	36			V
009	Vc()lo	Clamp Voltage lo at CQ, Q2 vs. VBO	I() = -1 mA, VBO > VN			-36	V
010	Vc()hi	Clamp Voltage hi at VN, VBO, VBR, CQ, Q2, CFI, VH, VHL vs. lowest voltage of VN, VBO, VBR, CQ, Q2, CFI, VH, VHL	I() = 1 mA	36			V
011	Vc()hi	Clamp Voltage hi at VSET, RX1, RX2, MISO	I() = 1 mA	7			V
012	Vc()lo	Clamp Voltage lo MOSI, SCK, NCS, TX1, TX2, VSET, OEN, RX1, RX2, NDIAG, MISO, VCC, VCC3, VHL	I() = -1 mA			-0.4	V
013	Vc()lo	Clamp Voltage lo at VH	I() = -4 mA	-1.9		-0.4	V
014	RGND	Resistance GND to VN			3	7	Ω
Low-Side Switch CQ, Q2							
101	Vs()lo	Saturation Voltage lo at CQ, Q2 vs. VN	OVLCx(2:0) = 101, VBO = 9...36 V; I() = 200 mA I() = 150 mA I() = 100 mA I() = 50 mA I() = 10 mA			 1.8 1.5 1.3 0.9 0.5	 V V V V V
102	Vs()lo	Saturation Voltage lo at CQ, Q2 vs. VN	OVLCx(2:0) = 101, VBO = 4.5...9 V; I() = 150 mA I() = 100 mA I() = 50 mA I() = 10 mA			 2.3 1.8 1.2 0.6	 V V V V
103	Isc()lo	Short-Circuit Current lo in CQ, Q2	V() = 3 V...VBO, VBO = 9...36 V; OVLCx(2:0) = 0x0 OVLCx(2:0) = 0x1 OVLCx(2:0) = 0x2 OVLCx(2:0) = 0x3 OVLCx(2:0) = 0x4 OVLCx(2:0) = 0x5	 55 80 110 140 170 210		 120 150 195 230 280 310	 mA mA mA mA mA mA
104	Vol()on	Overload Detection Threshold on	CQ, Q2 lo → hi, referenced to GND	2.2		3.5	V
105	Vol()off	Overload Detection Threshold off	CQ, Q2 hi → lo, referenced to GND	2.1		2.9	V
106	Vol()hys	Overload Detection Threshold Hysteresis	Vol()hys = Vol()on − Vol()off	0.1			V
107	SR()	Slew Rate (switch off → on)	VBO = 36 V, Cl = 2.2 nF, OVLCx(2:0) = 0x5; HSPx = 0; EXCHx = 0 HSPx = 1; EXCHx = 1	 60		45	 V/µs V/µs
108	Imax()	Maximum Current in CQ, Q2	OVLCx(2:0) = 0x7, V() > 3 V, VBO = 9...36 V	250	300	390	mA

ELECTRICAL CHARACTERISTICS

Operating Conditions: VBO = 4.5...36 V (referenced to VN), Tj = -40...125 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
109	Ir()	Reverse Current in CQ, Q2	Low side = on, V() = -6 V	-330			µA
110	Iexc()	Excitation Current	EXCx = 1, VBO = 9...36 V; HSPx = 0 (see Fig. 5) HSPx = 1 (see Fig. 5)	300		540 700	mA mA
111	texc	Excitation Time	EXCx = 1 (see Fig. 5), oscillator calibrated; TEXCx = 0 TEXCx = 1	2.2 6.7	2.5 7.5	2.7 8.1	µs µs
112	tdead	Dead Time	Push-pull configuration, low switch activation delay after high switch deactivation (see Fig. 4), oscilator calibrated; HSPx = 0 HSPx = 1		500 125	540 135	ns ns
113	Ilk()	Leakage Current at CQ, Q2	OEN = lo, EPUCF1 = 0, OVLCx(2:0) = 0x2; V(CQ, Q2) = VBO...VBO + 3 V, VBO = 4.5...33 V V(CQ, Q2) = 0...VBO V(CQ, Q2) = -6...0 V ; VBO = 0...36 V V(CQ, Q2) = VBO − 36 V...-3 V	0 -70 -90 -200		300 70 0 0	µA µA µA µA
High-Side Switch CQ, Q2							
201	Vs()hi	Saturation Voltage hi vs. VBO	OVLCx(2:0) = 101, VBO = 9...36 V; I() = -200 mA I() = -150 mA I() = -100 mA I() = -50 mA I() = -10 mA	-1.8 -1.5 -1.3 -0.9 -0.4			V V V V V
202	Vs()hi	Saturation Voltage hi vs. VBO	OVLCx(2:0) = 101, VBO = 4.5...9 V; I() = -150 mA I() = -100 mA I() = -50 mA I() = -10 mA	-2.3 -1.8 -1.2 -0.6			V V V V
203	Isc()hi	Short-Circuit Current hi	V() = 0 V...VBO − 3 V, VBO = 9...36 V; OVLCx(2:0) = 0x0 OVLCx(2:0) = 0x1 OVLCx(2:0) = 0x2 OVLCx(2:0) = 0x3 OVLCx(2:0) = 0x4 OVLCx(2:0) = 0x5	-120 -150 -195 -230 -280 -320		-55 -80 -100 -140 -170 -200	mA mA mA mA mA mA
204	Vol()on	Overload Detection Threshold on	CQ, Q2 hi → lo, referenced to VBO;	-3.9		-2.5	V
205	Vol()off	Overload Detection Threshold off	CQ, Q2 lo → hi, referenced to VBO;	-3.3		-2.1	V
206	Vol()hys	Overload Detection Threshold Hysteresis	Vol()hys = Vol()off − Vol()on	0.1			V
207	SR()	Slew Rate (switch off → on)	VBO = 36 V, Cl = 2.2 nF, OVLCx(2:0) = 0x5; HSPx = 0; EXCx = 0 HSPx = 1; EXCx = 1	35		40	V/µs V/µs
208	Imax()	Maximum Current in CQ, Q2	OVLCx(2:0) = 0x7, V() < VBO − 3 V, VBO = 9...36 V	-650		-250	mA
209	Ir()	Reverse Current in CQ, Q2	CQ, Q2 on, V() = VBO...VBO + 3 V, VBO = 4.5...33 V			300	µA
210	Iexc()	Excitation Current	EXCx = 1, VBO = 9...36 V; HSPx = 0 (see Fig. 5) HSPx = 1 (see Fig. 5)	-360 -700		-260	mA mA
211	texc	Excitation Time	EXCx = 1 (see Fig. 5), oscillator calibrated; TEXCx = 0 TEXCx = 1	2.2 6.7	2.5 7.5	2.7 8.1	µs µs
212	tdead	Dead Time	Push-pull configuration, high switch activation delay after low switch deactivation (see Fig. 4), oscillator calibrated; HSPx = 0 HSPx = 1		500 125	540 135	ns ns

ELECTRICAL CHARACTERISTICS

Operating Conditions: VBO = 4.5...36 V (referenced to VN), Tj = -40...125 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Short-Circuit/Overload Monitor/Wake-Up Request							
301	toldly	Time to Overload Message (OVLx 0 → 1, outputs tri-state)	Permanent overload (see Fig. 9)	126	160	213	µs
302	tolcl	Time to start retry (outputs active)		35	50	80	ms
303	toldrt	Time to Overload Message clearing (OVLx 1 → 0) during retry	No overload (see Fig. 10)		1		ms
304	tdscr	Time to Wake-Up Request acknowledge		73		87	µs
305	$tdnscr_{max}$	Maximum Time for no Wake-Up Request decision				60	µs
306	$tdnscr_{min}$	Minimum Time for no Wake-Up Request decision		110			µs
VBO Voltage Monitor							
401	VBOon	Turn-On Threshold VBO	Referenced to GND; UVTH(3:0) = 0x0 UVTH(3:0) = 0x4 UVTH(3:0) = 0xF	 3.5 8 17.7		 4.5 9 20	 V V V
402	VBOoff	Turn-Off Threshold VBO	Decreasing voltage VBO; UVTH(3:0) = 0x0 UVTH(3:0) = 0x4 UVTH(3:0) = 0xF	 3.5 7.3 17.5		 4.4 8.9 20	 V V V
403	VBOhys	Hysteresis	VBOhys = VBOon − VBOoff	50	500		mV
404	tUVB	UVBO flag persistence after event	No undervoltage at VBO		5		ms
405	tUVBFIL	VBO undervoltage detection filtering time	UVFIL = '0' UVFIL = '1'		0.1 1		ms ms
406	Vt()VNBR	NVBREV flag, autarchy monitor threshold, activated	VBR referenced to VBO	0.1		2	V
407	tVNBRFIL	Required event duration before setting VNBREV			10		µs
408	tVNBR	NVBREV flag persistence after event	VBR − VBO > VNBRth		5		ms
409	Ir(VBR)	Reverse Supply current from VBR to VBO	VBR − VBO > 1V			0.5	mA
410	C(VBR)	Maximum Capacitance at VBR			100		µF
Temperature Monitor							
501	Toff	Overtemperature Shutdown (TEMPOK 1 → 0, switch tri-state)	Increasing temperature Tj	140		175	°C
502	ton	Overtemperature Shutdown Reset Delay (TEMPOK 0 → 1, switch active)	Temperature Tj < Toff	35	50	80	ms
503	Trange	Temperature Digital Measurement Range		-40		125	°C
504	Tresol	Temperature Digital Measurement Resolution			1		°C
505	Reading	Temperature Value Ranges	Tj = 125 °C Tj = -40 °C	170 5		195 25	digits digits
Inputs TX1, TX2, MOSI, NCS, SCK, OEN							
601	Vt()hi	Input Threshold Voltage hi at TX1, TX2, MOSI, SCLK, OEN, NCS				1.7	V
602	Vt()lo	Input Threshold Voltage lo at TX1, TX2, MOSI, SCK, OEN, NCS		0.8			V
603	Vt()hys	Hysteresis at TX1, TX2, MOSI, SCK, OEN, NCS	Vt()hys = Vt()hi − Vt()lo	20	140		mV

ELECTRICAL CHARACTERISTICS

Operating Conditions: VBO = 4.5...36 V (referenced to VN), Tj = -40...125 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
604	Ipd()	Pull-Down Current at TX1, TX2, MOSI, SCK	V() = 0.4 V...VCC3	2		40	µA
605	Rpu()	Pull-up resistor at NCS	NCS to VCC3		100		kΩ
606	Ipd(OEN)	Pull-Down Current at OEN	V(OEN) = 0.4 V...VCC3	1		6	µA
607	tspu()	Permissible Spurious Pulse Width at TX1, TX2	No activity triggered, TXFIL(1:0) = 10			2.5	µs
608	ttrig()	Required Pulse Width at TX1, TX2	Activity triggered, TXFIL(1:0) = 10	6			µs
609	tspu()	Permissible Spurious Pulse Width at OEN	No activity triggered, OENFIL(1:0) = 10			5	µs
610	ttrig()	Required Pulse Width at OEN	Activity triggered, OENFIL(1:0) = 10	12			µs
611	tpio	Propagation Delay TX1 → CQ TX2 → Q2	TXFIL(1:0) = 10	2.4		10	µs
Diag Output NDIAG and MISO							
701	Vs()lo	Saturation Voltage lo at MISO, NDIAG	I() = 1.0 mA			0.4	V
702	Ilk()	Leakage Current in MISO	V() = 0 V...VCC, NCS = hi	-10		10	µA
703	Ilk()	Leakage Current in NDIAG	V() = 0 V...VCC, no error	-10		10	µA
704	Vs()hi	Saturation Voltage high at MISO	I(MISO) = -2 mA, Vs(MISO)hi = VCC3 − V(MISO)			0.4	V
705	Isc()hi	Short Circuit current hi in MISO	V(MISO) = 0...VCC3 − 0.4 V	-100			mA
706	Isc()lo	Short Circuit current lo in MISO	V(MISO) = 0.4 V...VCC3			100	mA
707	Isc()lo	Short Circuit current lo in NDIAG	V(NDIAG) = 0.4 V...VCC3			15	mA
708	tr(MISO)	Rise Time	Cl(MISO) = 30 pF, 0 → 90% VCC3			6	ns
709	tf(MISO)	Fall Time	100 → 10% VCC3			6	ns
Feedback Channel CQ, CFI to RX1, RX2							
801	Vt1()hi	Input Threshold 1 hi at CQ, CFI	VBO < 18 V	59	66	74	%VBR
802	Vt1()lo	Input Threshold 1 lo at CQ, CFI	VBO < 18 V	44	50	56	%VBR
803	Vt2()hi	Input Threshold 2 hi at CQ, CFI	VBO > 18 V	10.5	11.3	12.5	V
804	Vt2()lo	Input Threshold 2 lo at CQ, CFI	VBO > 18 V	8.3	9	10.5	V
805	Vt()hys	Hysteresis at CQ, CFI	Vt()hys = Vt()hi − Vt()lo	1			V
806	Ipu()	Pull-Up Current at CQ, CFI	EPUCFx = 1, PUNPDx = 1, V(CQ, CFI) = 0...VBO − 3 V; VBO = 4.5...9 V VBO = 9...36 V	 -370 -370		 -80 -120	 µA µA
807	Ipd()	Pull-Down Current at CQ, CFI	EPUCFx = 1, PUNPDx = 0, V(CQ,CFI) = 3 V...VBO; VBO = 4.5...9 V VBO = 9...36 V	 80 120		 370 370	 µA µA
808	tpcf	Propagation Delay CQ, CFI → RX1, RX2	V(RX1,RX2) = 10 ↔ 90%, RXFIL(1:0) = 01	2.4		10	µs
809	tsup()	Permissible Spurious Pulse Width at CQ,CFI	No activity triggered, RXFIL(1:0) = 01			2.5	µs
810	ttrig()	Required Pulse Width at CQ, CFI	Activity triggered, RXFIL(1:0) = 01	6			µs
811	Ipd(C)+ Ilk(Q2)	Pull-Down Current at CFI plus leakage current at Q2	V() = 3 V...VBO, OEN = lo, PUNPD2 = 0, EPUCF2 = 1	20			µA
812	Vs()hi	Saturation Voltage hi at RX1, RX2	I() = -2 mA, Vs()hi = VCC3 − V()			0.4	V
813	Vs()lo	Saturation Voltage low at RX1, RX2	I() = 2 mA			0.4	V
814	Isc()hi	Short Circuit current hi in RX1, RX2	V() = 0...VCC3 − 0.4 V	-40			mA
815	Isc()lo	Short Circuit current lo in RX1, RX2	V() = 0.4 V...VCC3			90	mA

ELECTRICAL CHARACTERISTICS

Operating Conditions: VBO = 4.5...36 V (referenced to VN), Tj = -40...125 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
816	tr()	Rise Time at RX1, RX2	CL() = 30 pF, 0 → 90% VCC3			22	ns
817	tf()	Fall Time at RX1, RX2	CL() = 30 pF, 100 → 10% VCC3			22	ns
Step Down Converter VHL, VH							
901	I(VH)max	Maximum current in VH	LVH = 100 µH, Ri(LVH) < 1.1 Ω, CVH = 10 µF; VHV(5:0) = 0x04..0x17 VHV(5:0) = 0x18..0x2C			 100 70	 mA mA
902	VHstep	VH configuration steps	Register VHV(5:0)		250		mV
905	VHn	Nominal Voltage at VH	LVH = 100 µH, Ri(LVH) < 1.1 Ω, CVH = 10 µF; VBO > 10 V: VHV(5:0) = 0x04, II = 0...100 mA VHV(5:0) = 0x0B, II = 0...100 mA VBO > (VH + 4 V): VHV(5:0) = 0x18, II = 0...70 mA VHV(5:0) = 0x2C, II = 0...70 mA	 4.7 6.3 9.5 14.3	 5 6.75 10 15	 5.4 7.5 10.5 15.6	 V V V V
906	VHnr	Nominal Voltage at VH, LVH replaced by a resistor	R = 170 Ω, I(VH) = 0...10 mA, VBO > 10 V, VHV(5:0) = 0x0B	6.3		8.4	V
907	Ia(VHL)	max. DC Cut-Off Current in VHL		-400		-120	mA
908	Va(VH)	Cut-Off Voltage at VH	Va(VH) > VHn; VHV(5:0) = 0x0B	6.5	7.3	8.4	V
910	Vs(VHL)	Saturation Voltage at VHL vs. VBR	I(VHL) = -50 mA I(VHL) = -150 mA		0.5 1.5	1.1 3.0	V V
911	Vf(VHL)	Saturation Voltage at VHL vs. GND	Vf(VHL) = V(GND) − V(VHL); I(VHL) = -50 mA I(VHL) = -150 mA		 0.6 1.7	 1.5 2.9	 V V
912	Ilk(VHL)	Leakage Current at VHL	VHL = Io, V(VHL) = V(VH)	-20		20	µA
913	ηVH	Efficiency of VH switching regulator	I(VH) = 50 mA, Ri(LVH) < 1.1 Ω, V(VBR) = 12...36 V	70*			%
Series Regulator VCC							
A01	VCCn	Nominal Voltage at VCC	I(VCC) = -50...0 mA, VH = VHn; VSET open, VH > 6.3 V VSET tied to VCC3 VSET tied to GND VSET tied to VCC	 4.5 3.0 2.3 1.6	 5 3.3 2.5 1.8	 5.5 3.6 2.7 2.0	 V V V V
A02	VCCdrop	Minimum voltage drop VH − VCC	EVCC = 1, VSET = open; I(VCC) = -10 mA I(VCC) = -50 mA	 0.75 1.25			 V V
A03	CVCC	Required Capacitor at VCC vs. GND		150			nF
A04	RiCVCC	Maximum Permissible Internal Resisitance of capacitor at VCC				1	Ω
A05	VCCon	VCC Monitor Threshold hi	Increasing Voltage at VCC; VSET open VSET tied to VCC3 VSET tied to GND VSET tied to VCC	 70 70 60 50		 98 98 98 98	 %VCCn %VCCn %VCCn %VCCn
A06	VCCoff	VCC Monitor Threshold lo	Decreasing Voltage at VCC; VSET open VSET tied to VCC3 VSET tied to GND VSET tied to VCC	 70 70 60 50		 95 95 95 95	 %VCCn %VCCn %VCCn %VCCn
A07	VCChys	Hysteresis	VCChys = VCCon − VCCoff	20	400		mV
A08	tUVCCFIL	VCC undervoltage detection filtering time	Continuous VCC undervoltage		30		µs
A09	tUVCC	UVCC flag persistence after event	No undervoltage at VCC		5		ms

* Projected values by sample characterization

ELECTRICAL CHARACTERISTICS

Operating Conditions: VBO = 4.5...36 V (referenced to VN), Tj = -40...125 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Series Regulator VCC3							
B01	VCC3n	Nominal Voltage at VCC3	I(VCC3) = -50...0 mA, VH = VHn	3.0	3.3	3.6	V
B02	CVCC3	Required Capacitor at VCC3 vs. GND		150			nF
B03	VCC3drop	Minimum voltage drop VH - VCC3	I(VCC3) = 0 mA I(VCC3) = -50 mA	0.4 1			V V
B04	RiCVCC3	Maximum Permissible Internal Resisitance of capacitor at VCC3				1	Ω
B05	VCC3on	VCC3 Monitor Threshold hi	Increasing Voltage at VCC3	2.3		3.0	V
B06	VCC3off	VCC3 Monitor Threshold lo	Decreasing Voltage at VCC3	2.0		2.8	V
B07	VCC3hys	Hysteresis	VCC3hys = VCC3on − VCC3off	50	450		mV
Oscillator							
C01	fos	Oscillator Frequency		7.35	8	8.83	MHz
SPI interface							
E01	tCSU	Chip select setup time	NCS stable low prior to SCLK rising edge	30			ns
E02	tCSH	Chip select hold time	NCS stable low after last SCLK falling edge	30			ns
E03	tCH	SCLK clock high time		31			ns
E04	tCL	SCLK clock low time		31			ns
E05	tSU	MOSI to clock setup time	MOSI stable before SCLK rising edge	4			ns
E06	tHO	MOSI to clock hold time	MOSI stabla after SCLK rising edge	15			ns
E07	tD	NCS high time	NCS stable at high after SPI communication	180			ns
E08	tMO	MISO valid time	MISO valid after SCLK falling edge, Cl $\leq$ 30 pF	0		25	ns
E09	tHIZ	MISO to HIZ time	MISO set to high impedance after NCS rising edge			160	ns
E10	fSCLK	SPI clock frequency				16	MHz

DESCRIPTION OF FUNCTIONS

iC-GFP has two independent switching channels which enable digital sensors to drive peripheral elements. They are designed to cope with high driver currents. The switches are reverse-polarity protected, feature a free-wheeling circuit for inductive loads and a saturation-voltage minimising system.

Reverse polarity protection

The pins VBO, CQ, Q2, VN, and CFI on the *line side* of the chip are reverse polarity protected. As far as the maximum voltage ratings are not exceeded, no possible supply combination at the *line side* pins can damage the chip.

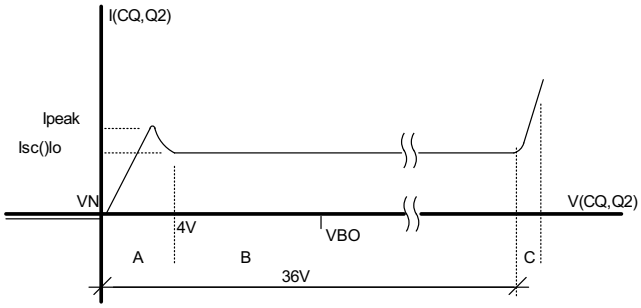


Figure 1: Low-side switch characteristic when active

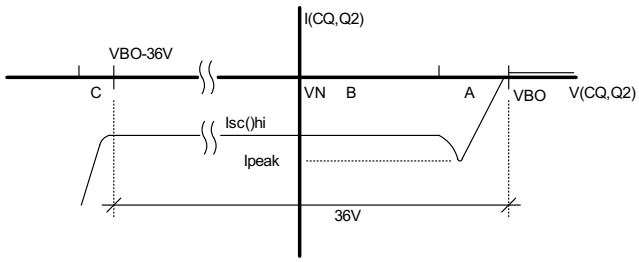


Figure 2: High-side switch characteristic when active

Output characteristics of CQ, Q2

The switching channels are current limited to a value set by the OVLCx bits. The current limitation works only for voltages higher than 4 V at the low-side switches or lower than VBO – 4 V at the high-side switches. For smaller output voltages the current limitation is disabled in order to minimise the saturation voltages without increasing the power dissipation. Figures 1 and 2 show the characteristic of the switching channels when activated. Region "A" is the saturation range, where the current limitation is not fully active yet and region "B" is the current limited range. Region "C" corresponds to the free-wheeling circuit activated. The switching channels are designed so that the low-side switches can only sink current and the high-side switches can only source current (no reverse current).

Free-wheeling circuit for inductive loads

The free-wheeling circuit is always present and does not depend on the output status. It is activated by voltages higher than 36 V at the low-side switches referenced to VN or lower than -36 V at the high-side switches referenced to VBO. In that case the corresponding channel will switch on without current limitation (see Figure 3).

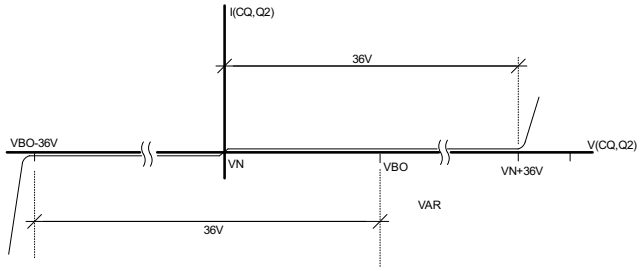


Figure 3: Free-wheeling characteristic

Dead time

In order to avoid current flow between high- and low-side switch in push-pull configuration, a dead time t_{dead} is implemented as shown in Figure 4 (cf. Electrical Characteristics Nos. 112 and 212).

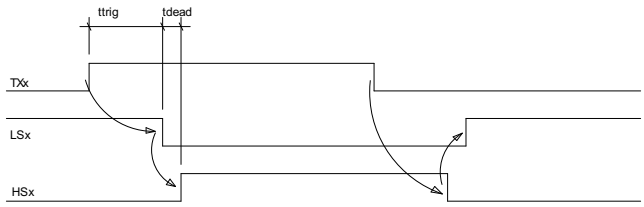


Figure 4: Propagation delay

Excitation current

With registers EXCx an additional current I_{exc} can be activated for driving capacitive loads. Figure 5 shows the characteristic of one channel with the excitation current enabled (cf. Electrical Characteristics Nos. 110, 111, 210 and 211). The excitation current duration is controlled by the TEXCx registers.

EXC1	Addr. 0x03; bit 3	R/W 0
0	CQ excitation current disabled	
1	CQ excitation current enabled	

Table 4: CQ excitation current selection

EXC2	Addr. 0x04; bit 3	R/W 0
0	Q2 excitation current disabled	
1	Q2 excitation current enabled	

Table 5: Q2 excitation current selection

TEXC1	Addr. 0x03; bit 6	R/W 0
0	CQ excitation current for typ. 2.5 µs	
1	CQ excitation current for typ. 7.5 µs	

Table 6: CQ excitation current duration

TEXC2	Addr. 0x04; bit 6	R/W 0
0	Q2 excitation current for typ. 2.5 µs	
1	Q2 excitation current for typ. 7.5 µs	

Table 7: Q2 excitation current duration

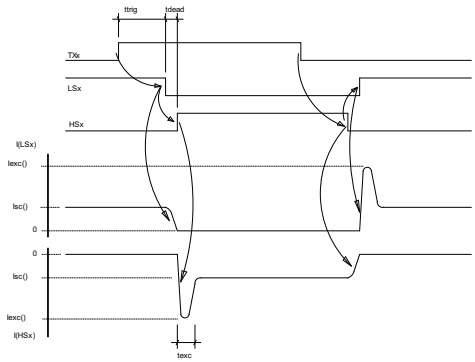


Figure 5: Excitation current

High speed mode
To meet the IO-Link COM3 requirements, the *High Speed* mode has to be enabled (HSPx). This mode increases the output current during communication.

HSP1	Addr. 0x03; bit 7	R/W 0
0	CQ set to normal speed mode	
1	CQ set to high speed mode	

Table 8: CQ High speed mode

HSP2	Addr. 0x04; bit 7	R/W 0
0	Q2 set to normal speed mode	
1	Q2 set to high speed mode	

Table 9: Q2 High speed mode

Switching converter with spread spectrum oscillator
The switching converter is controlled by VHDIS. The target voltage at VHL is set at VHV(5:0). To reduce the electromagnetic interference generated by the switching converter, a *spread spectrum oscillator* has been introduced. Here the switch is not triggered by a fixed frequency but by a varying 32-step frequency mix. Generated interference is thus distributed across the frequency spectrum with its amplitude reduced at the same time. This feature can be disabled via RNDDIS.

RNDDIS	Addr. 0x09; bit (7)	R/W 0
0	DC/DC converter noise spreading enabled	
1	DC/DC converter noise spreading disabled	

Table 10: DC/DC converter noise spreading

VHDIS	Addr. 0x09; bit (6)	R/W 0
0	DC/DC converter enabled	
1	DC/DC converter disabled	

Table 11: DC/DC converter disabling

VHV(5:0)	Addr. 0x09; bit (5:0)	R/W 001011
0x00	VH regulated to the min voltage	
...		
0x04	VH regulated to 5 V (cf. Electrical Characteristics No.905)	
...		
0x0B	VH regulated to 6.75 V (cf. Electrical Characteristics No.905)	
...		
0x18	VH regulated to 10 V (cf. Electrical Characteristics No.905)	
...		
0x2C	VH regulated to 15 V (cf. Electrical Characteristics No.905)	
...		
0x3F	Not supported	

Table 12: DC/DC converter output voltage

VCC3 regulator
The VCC3 regulator provides a 3.3 V voltage with up to 50 mA when VBR and VH are supplied. The VCC3 regulator supplies the digital circuitry of the chip. VBR and VH must be supplied for VCC3 operation.

VCC regulator
The VCC regulator is configured at VSET to 1.8, 2.5, 3.3, or 5 V output (cf. Electrical Characteristic No. A01) with up to 50 mA (see Table 13).

VCC voltage	VSET setting
1.8 V	shortcircuited to pin VCC
2.5 V	shortcircuited to pin GND
3.3 V	shortcircuited to pin VCC3
5 V	pin open

Table 13: VSET configuration for VCC regulator

The VSET pin is evaluated during the first 50 ms after power-up. Hence VSET must be stable longer than typ. 150 µs before the VCC regulator is switched to its operating point. After the first 50 ms have elapsed, changes at VSET don't affect the configuration. The configuration is redundantly stored and monitored for integrity to prevent undesired changes due interferences. For the 5 V configuration (VSET pin open), a 100 pF capacitor between VSET and GND is advised for additional filtering in noisy environments. Once the VCCOK status flag is cleared, the regulator is assumed to be correctly configured and its configuration can be read at SETV. VBR and VH must be supplied for VCC operation. The regulator can be disabled via EVCC.

SETV(1:0)	Addr. 0x00; bit 7:6	R
00	VCC regulator configured to 3.3 V	
01	VCC regulator configured to 5 V	
10	VCC regulator configured to 1.8 V	
11	VCC regulator configured to 2.5 V	

Table 14: SETV status

EVCC	Addr. 0x06; bit (6)	R/W 1
0	VCC regulator disabled	
1	VCC regulator enabled	

Table 15: VCC regulator control

Power Supply Rejection Ratio (PSRR)
Figures 6 to 8 show the power supply rejection ratio for different VH settings.

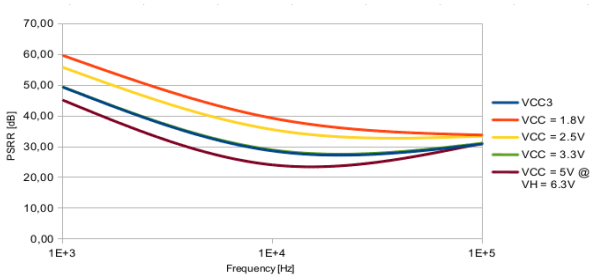


Figure 6: PSRR with VH = 4.5 V

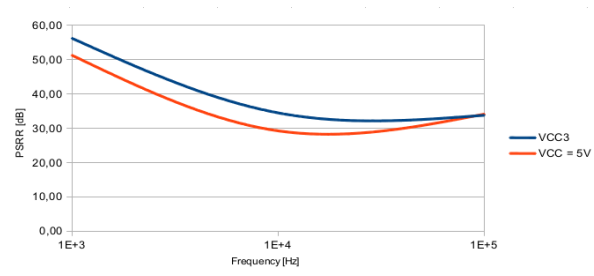


Figure 7: PSRR with VH = 8 V

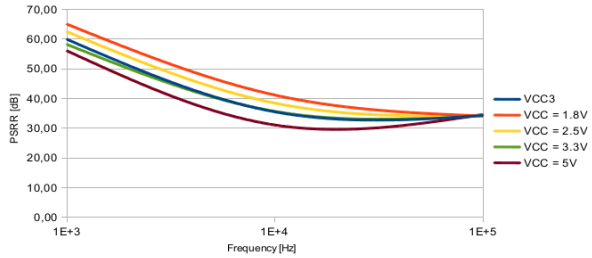


Figure 8: PSRR with VH = 24 V

Overload detection
To protect the device from excessive power dissipation due to high currents the switches are clocked, if an overload occurs. If a short circuit is detected, i.e. if the voltage at the switch output overshoots or undershoots *Overload Detection Threshold off* (cf. Electrical Characteristics Nos. 105 and 205), the switches are shut down for typ. 50 ms (cf. Electrical Characteristics No. 302).

The level of power dissipation depends on the current and the time during which this current flows. A current which fails to trigger the overload detection is not critical; high current can also be tolerated for a short period and with low repetition rates. This is particularly important when switching capacitive loads (charge/discharge currents).

There are two overload detection modes. In Normal Overload Detection Mode (SOVL = 0), overload is detected only when the switches are continously overloaded for longer than typical 160 µs (cf. Electrical Characteristics No. 301).

SOVL	Addr. 0x06; bit 6	R/W 1
0	Normal overload detection mode	
1	Smart overload detection mode	

Table 16: Overload mode configuration

In Smart Overload Detection Mode (SOVL = 1, iC-GF legacy mode) two back-end integrators follow the switches for the purpose of overload detection. Each integrator is a counter which is updated together with the on-chip clock. If an overload is detected at one channel the respective counter is incremented. If no overload is apparent, the counter is decremented after a certain time. This time is controlled by the DTY1(1:0) and DTY2(1:0) for channel CQ and Q2 respectively.

DTY1(1:0)	Addr. 0x03; bit (5:4)	R/W 10
00	Duty cycle of 1:4	
01	Duty cycle of 1:8	
10	Duty cycle of 1:10	
11	Duty cycle of 1:15	

Table 17: Overload detection duty cycle for CQ

DTY2(1:0)	Addr. 0x04; bit (5:4)	R/W 10
00	Duty cycle of 1:4	
01	Duty cycle of 1:8	
10	Duty cycle of 1:10	
11	Duty cycle of 1:15	

Table 18: Overload detection duty cycle for Q2

When the counter reaches the overload level, the corresponding output switch is shut down for typical 50 ms which is signaled by clearing NOVL1, NOVL2. This will also be signaled at output pin NDIAG. Setting MOVL to 1 suppresses the signaling at NDIAG.

MOVL	Addr. 0x08; bit 4	R/W 1
0	NOVLx will not be signaled at NDIAG	
1	NOVLx will be signaled at NDIAG	

Table 19: Overload signaling mask

Thus the switches can be overloaded with a certain duty cycle.

After the 50 ms switches shut down time has elapsed, the iC-GFP tries to enable the switches again while keeping the overload signals. After typical 1 ms (cf. Electrical Characteristics No. 303) the switches are released for normal operation and if no new overload is detected within this time, the corresponding NOVL1/NOVL2 status bit is the set.

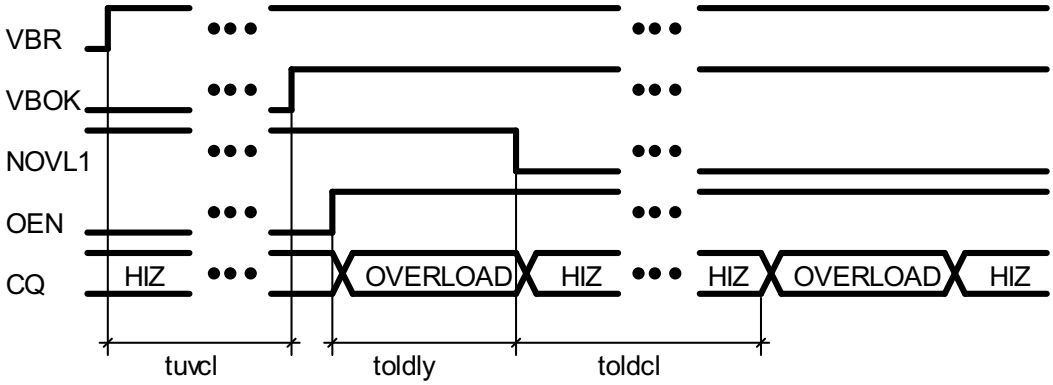


Figure 9: Permanent short circuit at channel CQ

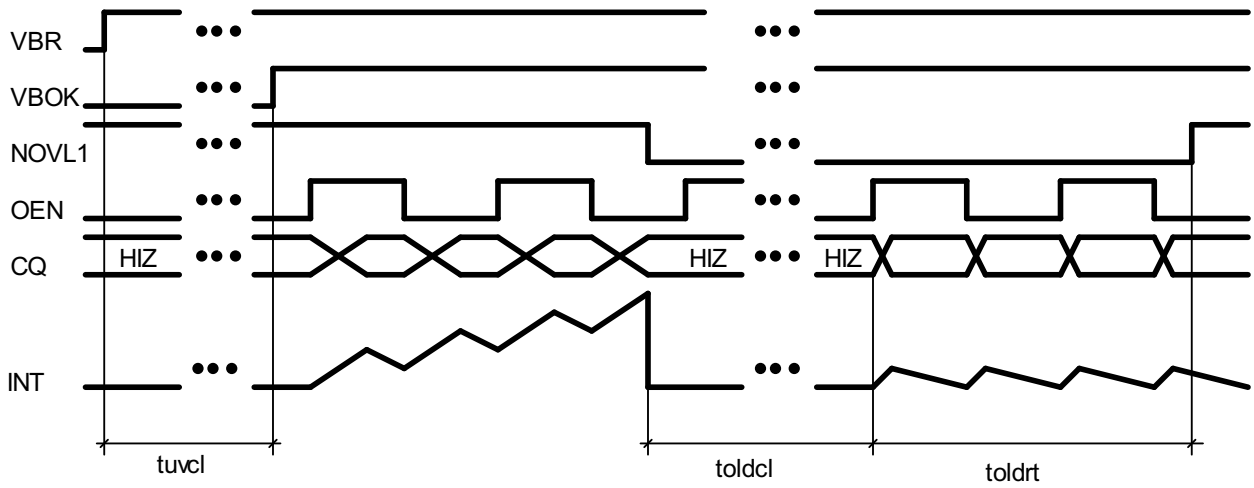


Figure 10: Temporal short circuit at channel CQ

Switching channels CQ, Q2

iC-GFP implements two independent switching channels, CQ and Q2. Both channels have configurable digital filters, configurable polarity, and can be output at either output pin (cf. Figure 11).

OEN1	Addr. 0x01; bit 1	R/W 0
0	Channel CQ forced to HIZ (depends on IFOEN)	
1	Channel CQ enabled (depends on IFOEN)	

Table 20: OEN1

Each switching channel can be disabled (forced to HIZ) by setting the corresponding OENx bit to 0 or by pulling the OEN pin low. The OEN pin may be configured to control any, both or none of the channels.

OEN2	Addr. 0x01; bit 4	R/W 0
0	Channel Q2 forced to HIZ (depends on IFOEN)	
1	Channel Q2 enabled (depends on IFOEN)	

Table 21: OEN2

IFOEN(1:0)	Addr. 0x06; bit (4:3)	R/W 11
00	OEN has no effect; CQ, Q2 controlled by corresponding OENx bit	
01	OEN controls only CQ; OEN1 bit has no effect	
10	OEN controls only Q2I; OEN2 bit has no effect	
11	OEN controls CQ and Q2; OEN1 and OEN2 bits have no effect	

Table 22: OEN pin configuration

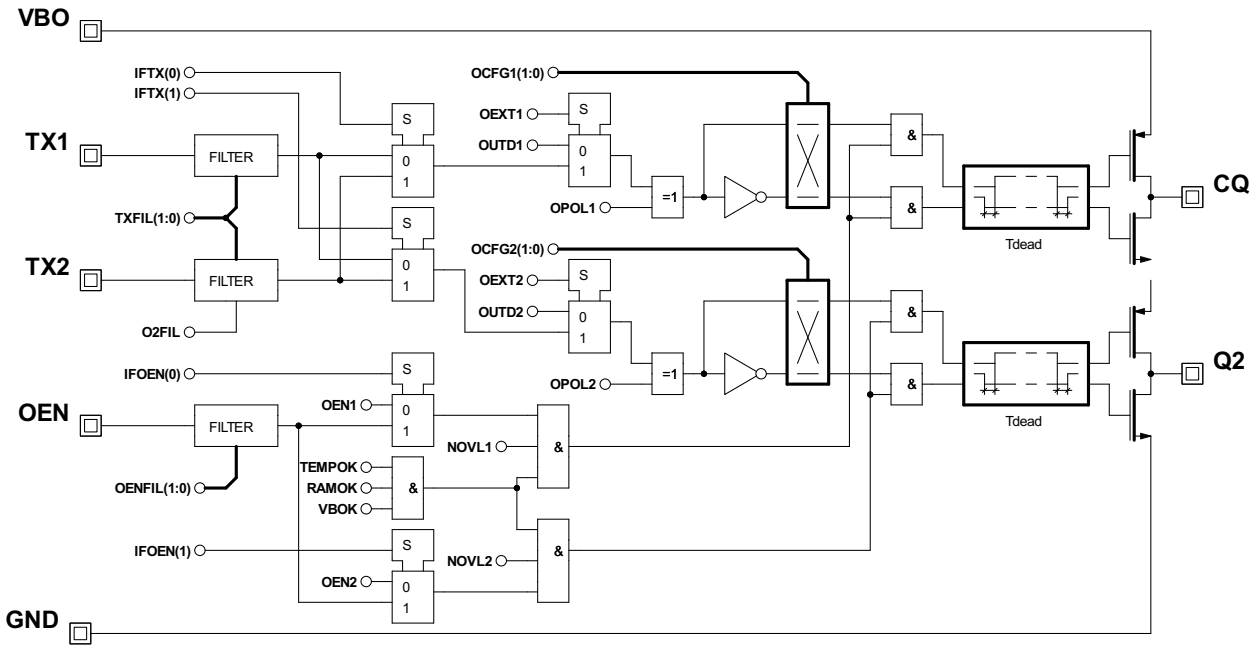


Figure 11: Output channels equivalent logic

The input pins TX1, TX2 and OEN are digitally filtered as per the Tables below.

TXFIL(1:0)	Addr. 0x07; bit (1:0)	R/W 10
00	Filter disabled	
01	1 µs filter	
10	4 µs filter	
11	7 µs filter	

Table 23: TX1, TX2 filter configuration

O2FIL	Addr. 0x06; bit 5	R/W 1
0	Filter at TX2 disabled	
1	Filter at TX2 enabled and controlled by TXFIL	

Table 24: TX2 filter disable

OENFIL(1:0)	Addr. 0x07; bit (7:6)	R/W 10
00	Filter disabled	
01	3 µs filter	
10	8 µs filter	
11	15 µs filter	

Table 25: OEN pin filter configuration

OUTD1	Addr. 0x01; bit 0	R/W 0
0	Channel CQ activated (controlled by OPOL1 and OCFG1)	
1	Channel CQ deactivated (controlled by OPOL1 and OCFG1)	

Table 26: OUTD1

If enabled, each channel may be controlled by bit OUTD1 for CQ and OUTD2 for Q2 or by pin TX1 and TX2. OEXT1 and OEXT2 select, if the channels are controlled by bit or by pin (see Fig. 11).

OUTD2	Addr. 0x01; bit 3	R/W 0
0	Channel Q2 activated (controlled by OPOL1 and OCFG1)	
1	Channel Q2 deactivated (controlled by OPOL1 and OCFG1)	

Table 27: OUTD2

OEXT1	Addr. 0x01; bit 2	R/W 0
0	Channel CQ controlled by OUTD1 bit	
1	Channel CQ controlled by TX pin (depends on IFTX)	

Table 28: OEXT1

OEXT2	Addr. 0x01; bit 5	R/W 0
0	Channel Q2 controlled by OUTD2 bit	
1	Channel Q2 controlled by TX pin (depends on IFTX)	

Table 29: OEXT2

OCFG1	Addr. 0x02; bit (1:0)	R/W 11
00	CQ set to HIZ	
01	CQ configured as low-side driver	
10	CQ configured as high-side driver	
11	CQ configured as push-pull driver	

Table 30: CQ configuration

OCFG2	Addr. 0x02; bit (5:4)	R/W 11
00	Q2 set to HIZ	
01	Q2 configured as low-side driver	
10	Q2 configured as high-side driver	
11	Q2 configured as push-pull driver	

Table 31: Q2 configuration

Both TX1 and TX2 can be selected to control any of the two channels.

IFTX(1:0)	Addr. 0x06; bit (1:0)	R/W 10
00	CQ and Q2 controlled by TX1; TX2 has no effect	
01	CQ controlled by TX2; Q2 controlled by TX1	
10	CQ controlled by TX1; Q2 controlled by TX2	
11	CQ and Q2 controlled by TX2; TX1 has no effect	

Table 32: TX1, TX2 configuration

The polarity of the switching channels can be inverted with the OPOL1 for CQ and OPOL2 for Q2.

OPOL1	Addr. 0x02; bit 2	R/W 0
0	CQ not inverted	
1	CQ inverted	

Table 33: CQ output polarity

OPOL2	Addr. 0x02; bit 6	R/W 0
0	Q2 not inverted	
1	Q2 inverted	

Table 34: Q2 output polarity

CHANNEL CQ					
OEXT1	OCFG1	TX1	OUTD1	OPOL1	CQ
X	00	x	X	X	HIZ
0	01	x	0	0	HIZ
0	01	x	0	1	0
0	01	x	1	0	0
0	01	x	1	1	HIZ
0	10	x	0	0	HIZ
0	10	x	0	1	1
0	10	x	1	0	1
0	10	x	1	1	HIZ
0	11	x	0	0	0
0	11	x	0	1	1
0	11	x	1	0	1
0	11	x	1	1	0
1	01	L	x	0	HIZ
1	01	L	x	1	0
1	01	H	x	0	0
1	01	H	x	1	HIZ
1	10	L	x	0	HIZ
1	10	L	x	1	1
1	10	H	x	0	1
1	10	H	x	1	HIZ
1	11	L	x	0	0
1	11	L	x	1	1
1	11	H	x	0	1
1	11	H	x	1	0

Table 35: Function table for channel CQ, OEN pin = hi, IFOEN = 11, CQ = 0 = low-side switch on, CQ = 1 = high-side switch on, CQ = HIZ = both switches off

Synchronized outputs

With SYNC = hi output Q2 is in sync with CQ. All configurations for Q2 are ignored except for OPOL2, allowing an anvialent output. In case of an overload of any of the channels, both CQ and Q2 will be set to HIZ and only the flag (NOVL1, NOVL2) corresponding to the channel with the overload will be cleared.

SYNC	Addr. 0x02; bit 7	R/W 0
0	Synchronized outputs disabled	
1	Synchronized outputs enabled (depends on OPOL2)	

Table 36: Synchronized outputs

Feedback channels configuration
iC-GFP features two feedback channels. Channel 1 is internally connected to CQ and channel 2 controlled by pin CFI. Both channels feature configurable digital filters, an input polarity selection, and can be output at either RX1 and RX2 (cf. Figure 12).

ENCF1	Addr. 0x05; bit 0	R/W 0
0	CQ feedback channel disabled	
1	CQ feedback channel enabled	

Table 37: CQ feeback channel enable

ENCF2	Addr. 0x05; bit 4	R/W 0
0	CFI feedback channel disabled	
1	CFI feedback channel enabled	

Table 38: CFI feeback channel enable

IFRX	Addr. 0x06; bit (2)	R/W 0
0	RX1 controlled by CQ; RX2 controlled by CFI	
1	RX1 controlled by CFI; RX2 controlled by CQ	

Table 39: RX1, RX2 pins configuration

Both input pins, CFI and CQ, are digitally filtered. These filters are configured as per the Tables below.

CQFIL(1:0)	Addr. 0x07; bit (3:2)	R/W 01
00	Filter disabled	
01	4 µs filter	
10	7 µs filter	
11	16 µs filter	

Table 40: CQ feedback channel filter configuration

CFIFIL(1:0)	Addr. 0x07; bit (5:4)	R/W 01
00	Filter disabled	
01	4 µs filter	
10	7 µs filter	
11	16 µs filter	

Table 41: CFI feedback channel filter configuration

The polarity of the feedback channel CQ → RX1 and CFI → RX2 can be configured by CFPOL1 and CFPOL2.

CFPOL1	Addr. 0x05; bit 1	R/W 0
0	CQ hi → RX1 hi	
1	CQ hi → RX1 lo	

Table 42: CQ input polarity

CFPOL2	Addr. 0x05; bit 5	R/W 0
0	CFI hi → RX2 hi	
1	CFI hi → RX2 lo	

Table 43: CFI input polarity

The pull-up/down current at the inputs can be changed in polarity or disabled by means of EPUCF1, EPUCF2, PUNPD1, and PUNPD2.

EPUCF1	Addr. 0x05; bit 2	R/W 1
0	CQ pull-up/down disabled	
1	CQ pull-up/down enabled	

Table 44: Enable pull-up/down CQ

EPUCF2	Addr. 0x05; bit 6	R/W 1
0	CFI pull-up/down disabled	
1	CFI pull-up/down enabled	

Table 45: Enable pull-up/down CFI

PUNPD1	Addr. 0x05; bit 3	R/W 0
0	Pull-down current	
1	Pull-up current	

Table 46: Current polarity at CQ

PUNPD2	Addr. 0x05; bit 7	R/W 0
0	Pull-down current	
1	Pull-up current	

Table 47: Current polarity at CFI

The state of CQ and CFI (high or low) after the selected polarity inversion is mapped to IND1 and IND2.

IND1	Addr. 0x01; bit 6	R
0	Signal at CQ is low	
1	Signal at CQ is high	

Table 48: CQ status

IND2	Addr. 0x01; bit 7	R
0	Input Signal at CFI is low	
1	Input Signal at CFI is high	

Table 49: CFI status

Any change at CQ or CFI causes NCI1 (for CQ) or NCI2 (for CFI) to be set to 0. The flags are reset back to 1 after being read.

NCI1	Addr. 0x00; bit 2	R
0	CQ changed its value at least once since last read	
1	CQ didn't change its value since last read	

Table 50: NCI1 status bit

NCI2	Addr. 0x00; bit 3	R
0	CFI changed its value at least once since last read	
1	CFI didn't change its value since last read	

Table 51: NCI2 status bit

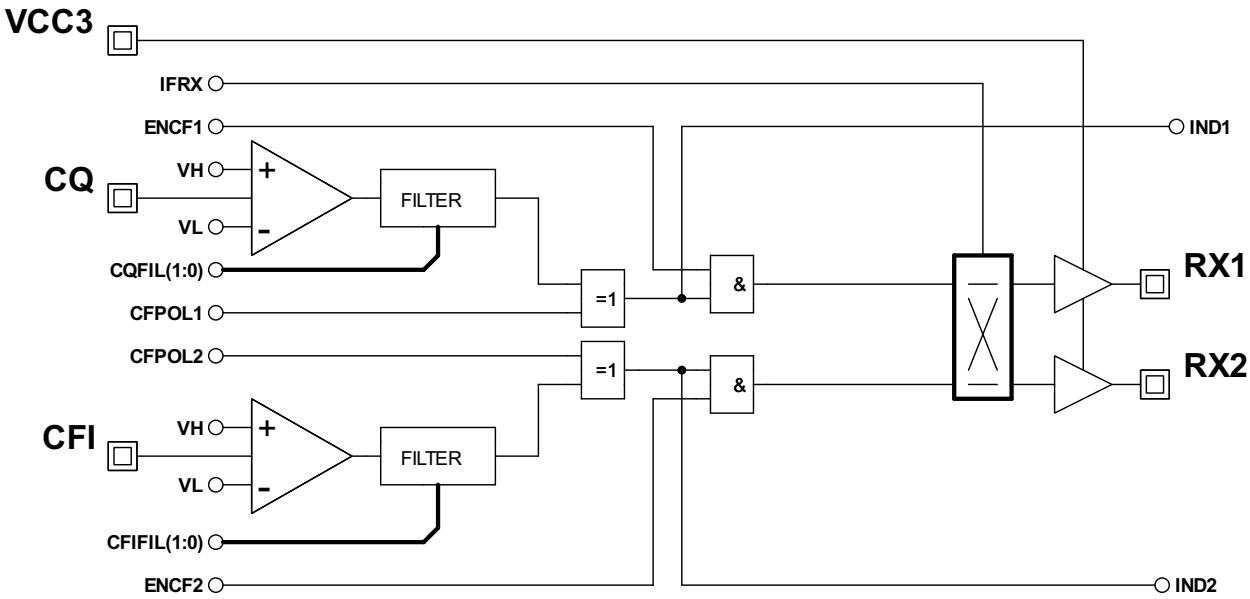


Figure 12: Feedback channels equivalent logic

Feedback channel CFI					
CFI	CFPOL2	PUNPD2	IND2	RX2	Current at CFI
0	0	0	0	0	down
1	0	0	1	1	down
0	1	0	1	1	down
1	1	0	0	0	down
0	0	1	0	0	up
1	0	1	1	1	up
0	1	1	1	1	up
1	1	1	0	0	up

Table 52: Function table of feedback channel CFI (EPUCF2 = 1, IFRX = 0, ENCF2 = 1)

IO-Link wake-up request detection
iC-GFP can detect an IO-Link wake-up request on either CQ or Q2. WUS selects the source. When WUS is set to hi, Q2 must be externaly tied to CFI. The feedback channel must be enabled for wake-up detection by ENCF1 or ENCF2.

WUS	Addr. 0x02; bit 3	R/W 0
0	CQ is the source channel for wake-up	
1	CFI is the source channel for wake-up	

Table 53: Wake-up source channel

ENCF1	Addr. 0x05; bit 0	R/W 0
0	CQ feedback channel disabled	
1	CQ feedback channel enabled	

Table 54: CQ feeback channel enable

A wake-up is generated by pulling the source channel for typ. 80 µs (cf. Electrical Characteristics No. 304) to a contrasting level (cf. Tables 58 and 59). The output enable pin and bits do not affect the wake-up polarity. Once the wake-up request is acknowledged, NWUD is cleared and if the error mask MWUD is set to hi, pin NDIAG will be set to lo as an interrupt for the MCU.

ENCF2	Addr. 0x05; bit 4	R/W 0
0	CFI feedback channel disabled	
1	CFI feedback channel enabled	

Table 55: CFI feeback channel enable

NWUD	Addr. 0x00; bit 0	R
0	At least one wake-up event occurred since last read	
1	No wake-up event occurred since last read	

Table 56: NWUD status bit

MWUD	Addr. 0x08; bit (0)	R/W 1
0	NWUD will not be signaled at NDIAG	
1	NWUD will be signaled at NDIAG	

Table 57: Wake-up signaling mask

NWUD is reset to hi after reading the status register.

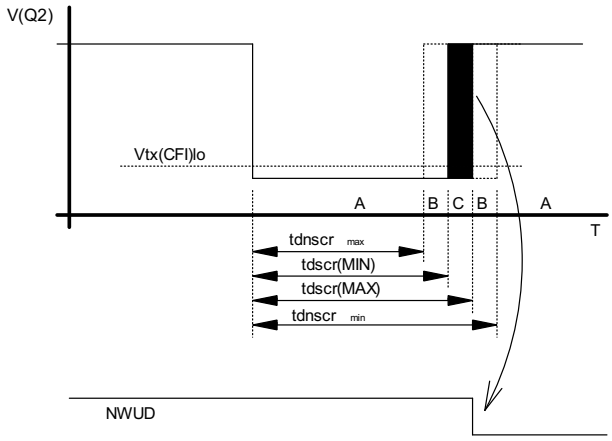


Figure 13: Wake-up request timing:
A: Wake-up request ignored
B: Uncertainty range
C: Wake-up request acknowledged

Wake-up request at CQ			
OUTD/TX (as selected)	OCFG1(1:0)	Expected CQ level	CQ pulse (70...90 µs)
0	11 push-pull	lo	hi
1	11 push-pull	hi	lo
0	10 high-side	lo	hi
1	10 high-side	hi	lo
0	01 low-side	hi	lo
1	01 low-side	lo	hi

Table 58: Communication request at CQ, WUS = 0, ENCF1 = 1, OPOLx = 1

Wake-up request at Q2			
OUTD/TX (as selected)	OCFG2(1:0)	Expected Q2 level	Q2 pulse (70...90 µs)
0	11 push-pull	lo	hi
1	11 push-pull	hi	lo
0	10 high-side	lo	hi
1	10 high-side	hi	lo
0	01 low-side	hi	lo
1	01 low-side	lo	hi

Table 59: Communication request at Q2, WUS = 1, ENCF2 = 1, OPOLx = 0, Q2 tied to CFI

On-chip temperature sensor

TCUR(7:0)	Addr. 0x0C; bit (7:0)	R
0x00	-56 °C	
...		
0xFE	198 °C	
0xFF	Invalid measure	

Table 60: Temperature sensor reading

An 8-bit digital temperature sensor can be read at address TCUR(7:0). A temperature alarm can be set TSET(7:0). If the measured temperature exceedes the value stored at TSET(7:0), NTWRN is cleared. Depending on the state of the mask bit MNTWRN, this will also be signaled at pin NDIAG. After power-up, during the first 50 ms and in case of overtemperature, temperature sensor readout is considered to be inaccurate and therefore marked as invalid (output 0xFF) and no temperature alarm will be generated.

TSET(7:0)	Addr. 0x0B; bit (7:0)	R/W 11111111
0x00	Alarm threshold set to TCUR = 0x00	
...		
0xFF	Alarm threshold set to TCUR = 0xFF	

Table 61: Overtemperature alarm threshold

MNTWRN	Addr. 0x08; bit (1)	R/W 1
0	NTWRN will not be signaled at NDIAG	
1	NTWRN will be signaled at NDIAG	

Table 62: Overtemperature signaling mask

POWER-UP AND POWER DOWN

There are 4 monitored supply voltages: VCC3, VCC, VBO and autarchy (V(VBO) – V(VBR)).

VCC3 monitor

With undervoltage at VCC3 (cf. Electrical Characteristics Nos. B05 and B06), the RAM and the SPI interface are reset. No communication is possible. With undervoltage removed, the RAMOK flag is cleared and can only be set by explicitly reading the RAM adress 0x0F. The content of this register is also output at each start of SPI comunication. This type of access though will not set or reset any status flags. While RAMOK is cleared, pin NDIAG will remain low and the output channels disabled. This cannot be masked. After power-up, the outputs stay disabled for typ. 50 ms. During this time the status bit OENST will be cleared.

VCC monitor

VCC undervoltage levels depend on the selected configuration of the regulator at pin VSET (5 V, 3.3 V, 2.5 V or 1.8 V) and if the regulator is enabled via EVCC (cf. Electrical Characteristics Nos. A05 and A06). VCC undervoltage will be signaled by clearing VCCOK, if the undervoltage persists longer than typ. 30 µs. VCCOK remains low for typ. 5 ms after undervoltage is removed. While VCCOK is cleared, diagnostic pin NDIAG will remain low. This can be suppressed by clearing MUVD.

EVCC	Addr. 0x06; bit (6)	R/W 1
0	VCC regulator disabled	
1	VCC regulator enabled	

Table 63: VCC regulator control

VCCOK	Addr. 0x0F; bit 4	R
0	VCC voltage lower than threshold	
1	VCC voltage higher than threshold	

Table 64: VCCOK status bit

MUVD	Addr. 0x08; bit 5	R/W 1
0	VCCOK will not be signaled at NDIAG	
1	VCCOK will be signaled at NDIAG	

Table 65: VCC Undervoltage signaling mask

VBO monitor

VBO undervoltage levels depend on the selected configuration in UVTH (cf. Electrical Characteristics Nos. 401 and 402). VBO undervoltage will be signaled by clearing VBOK, if undervoltage persists longer than the selected filter time (UVFIL). VBOK remains low for typ. 5 ms after undervoltage is removed. While VBOK is cleared, diagnostic pin NDIAG will remain low and the output channels disabled. This cannot be masked.

UVFIL	Addr. 0x0A; bit (4)	R/W 0
0	VBO undervoltage filter set to typ. 0.1 ms	
1	VBO undervoltage filter set to typ. 1 ms	

Table 66: VBO undervoltage filter configuration

VBOK	Addr. 0x0F; bit 5	R
0	VBO voltage lower than selected threshold (UVTH)	
1	VBO voltage higher than selected threshold (UVTH)	

Table 67: VBOK status bit

UVTH(3:0)	Addr. 0x0A; bit (3:0)	R/W 0100
0x0	VBO undervoltage setpoint to 4.5 V	
0x1	VBO undervoltage setpoint to 6 V	
0x2	VBO undervoltage setpoint to 7 V	
0x3	VBO undervoltage setpoint to 8 V	
0x4	VBO undervoltage setpoint to 9 V	
0x5	VBO undervoltage setpoint to 10 V	
0x6	VBO undervoltage setpoint to 11 V	
0x7	VBO undervoltage setpoint to 12 V	
0x8	VBO undervoltage setpoint to 13 V	
0x9	VBO undervoltage setpoint to 14 V	
0xA	VBO undervoltage setpoint to 15 V	
0xB	VBO undervoltage setpoint to 16 V	
0xC	VBO undervoltage setpoint to 17 V	
0xD	VBO undervoltage setpoint to 18 V	
0xE	VBO undervoltage setpoint to 19 V	
0xF	VBO undervoltage setpoint to 20 V	

Table 68: VBO undervoltage configuration.

Autarchy monitor V(VBO) – V(VBR)
The voltage at VBO compared to VBR can be used to detect e.g. a faulty VBO connection (a broken wire). If VBO is typ. 0.5 V below VBR for more than typ. 8 µs, NVBREV will be cleared. NVBREV remains low for typ. 5 ms after after this condition has been removed. While NVBREV is cleared, diagnostic pin NDIAG will remain low. This can be suppressed by clearing MNVBREV.

NVBREV	Addr. 0x0F; bit 3	R
0	VBO voltage lower than VBR	
1	VBO voltage higher or equal to VBR	

Table 69: NVBREV status bit

RAMOK	Addr. 0x0F; bit 7	R
0	RAM memory initialized; CQ, Q2 forced to HIZ	
1	RAM memory not initialized since last read	

Table 70: RAMOK status bit

OENST	Addr. 0x00; bit 4	R
0	CQ, Q2 forced to HIZ due to chip status (VBOK, TEMPOK, RAMOK, power-up delay, overload)	
1	CQ, Q2 released for user control	

Table 71: OENST status bit

Monitor	Status	Filter	Persistence	Comments
V(VCC3)	RAMOK	< 1 µs	until read	CQ, Q2 disabled, RAM reset
V(VCC)	VCCOK	30 µs	5 ms	No effect on chip functions
V(VBO)	VBOK	100...200 µs	5 ms	CQ, Q2 disabled
V(VBO) – V(VBR)	NVBREV	5 µs	5 ms	No effect on chip functions

Table 72: Overview of the supply monitors

Power-up sequence
A typical power-up sequence assuming VH = VBR is:

1. **VBO < 4.5 V:** The chip is in power-down state, no communication is possible. MISO is kept lo. The controller can tell the chip is in power-down by polling the STATUSF register at 0x0F which reads 0x00 (MISO = lo).
2. **VBO increases above 4.5 V:** The VCC3 regulator is operative and once its nominal value is reached, the chip enters the power-up state. Communication is now possible and the controller can now get a valid STAUSF reading. VBO and VCC undervoltage are assumed to have occured during VCC3 power-down and therefore the corresponding flags are cleared. VBO remains not OK since the default configuration for UVTH is 8 V. A typical first reading of STATUSF after power-up is 0x47 (RAMOK = 0, COMOK = 1, VBOK = 0, VCCOK = 0, NVBREV = 1, TEMPOK = 1, NOVL2 = 1, NOVL2 = 1). Immediatly after power-up, a 50 ms timer starts. During this time the output channels are disabled and set to HIZ. This is signaled at OENST which indicates that the output channels have been disabled by the internal logic (not by the user).
3. **VCC regulator reaches the configured value:** Once the VCC3 regulator is OK, the configuration at VSET is read and the VCC regulator enabled. After the set voltage level is reached, the VCCOK flag remains cleared for about 5 ms.
4. **VBO increases above the default undervoltage threshold (about 9 V):** Once VBO undervoltage is removed VBOK remains cleared for about 5 ms.
5. **Release of the output channels:** After VCC3 and VBO levels are OK, all of the following conditions must be ensured for the output channels to be released:
   - 50 ms power-up timer is elapsed
   - 5 ms VBOK persistence is elapsed
   - RAMOK flag has been read
   - No other condition has ocurred that leads to output disabling such as overload or overtemperature

Figure 14 ilustrates this sequence.

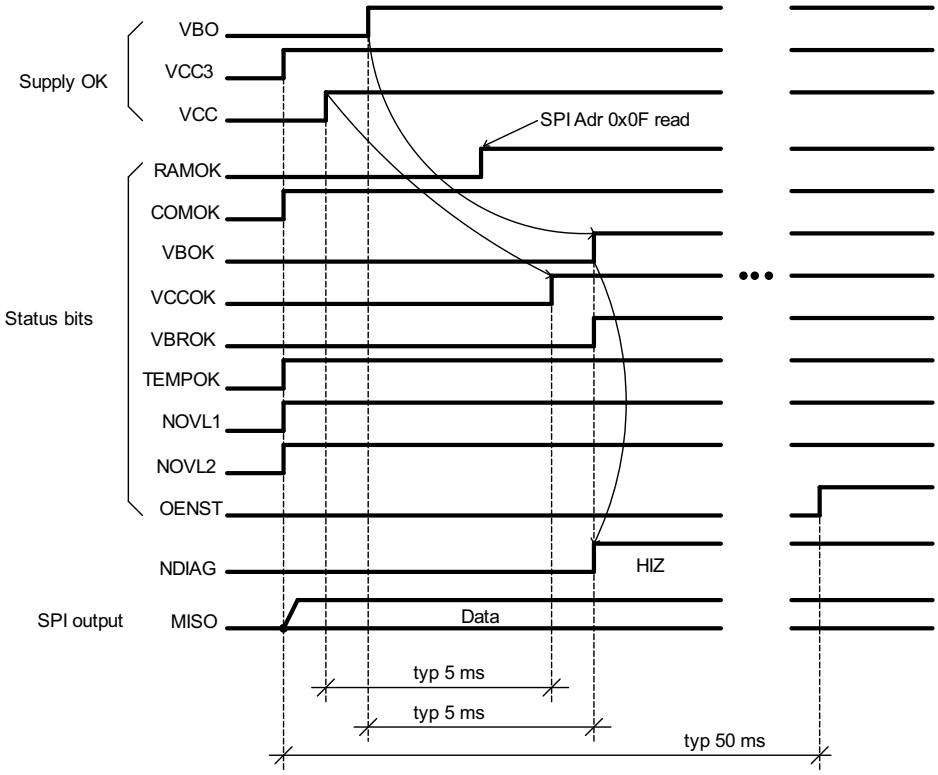


Figure 14: Typical power-up sequence

SPI INTERFACE WITH SECURED TRANSMISSION

Secured data transmission
The configuration RAM is secured against communication errors during data write such as clock injection or data corruption and permits atomic application of the configuration (all registers changed at once). Data is bytewise loaded into the RAM and may be automatically read back for data corruption monitoring. During this process iC-GFP keeps the last valid configuration, avoiding intermediate configuration states. Once the configuration data is read back and checked, it can be validated and applied to the system.

The data validation method is implemented with RAM and latch registers. The SPI write commands insert data into the RAM, but this RAM is only applied to the configuration registers once it has been validated (see Fig. 15).

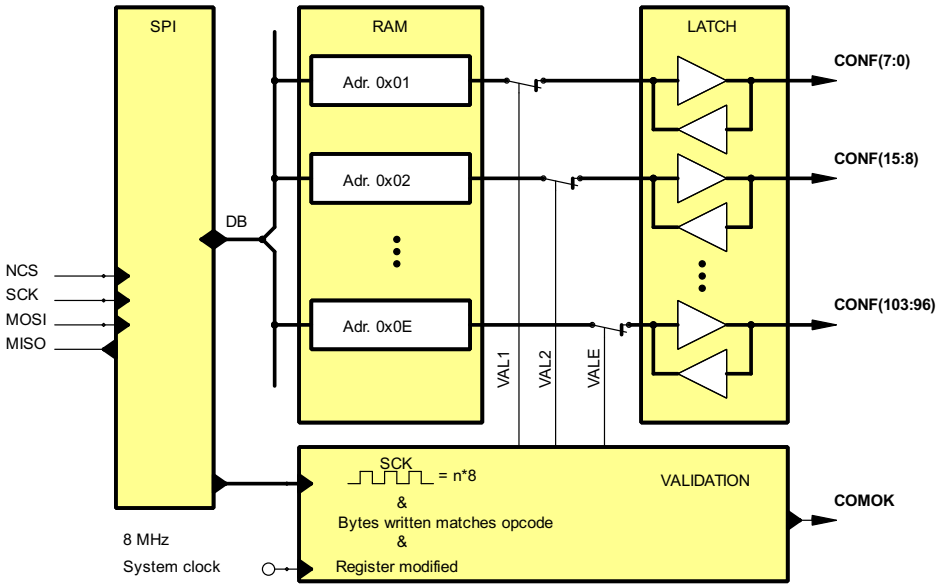


Figure 15: SPI secured transmission principle

An SPI command consists of an NCS falling edge, a first frame containing the operation code (OPC) and the start address, the corresponding data bytes in case of a write command or the required clock pulses to shift data out in case of a read command. Every input at MOSI will be output at MISO with an 8 clocks delay. This allows the MCU to check the sent data prior to its validation and to detect transmission errors. After the falling edge at NCS, the first data to be output is the chip status wich is stored at the address 0x0F (= STATUSF). Note: The status bits will be output but errors bits will not be cleared. To clear errors bits, for example RAMOK, it is required to explicitly read the relevant registers.

The operation code, OPC, selects the type of access (read or write) and in case of a write, the number of bytes to be written.

OPC(3:0)	Operation	Comment
0x0	Read	Standard SPI read
0x1..0xE	Write the corresponding number of bytes	Write with validation
0xF	Write standard SPI	Standard SPI write

Table 73: SPI Operation code meaning

Read commands
The operation code 0x0 can be used to read the contents of the configuration register. The first address to be read must be indicated in the first byte following the operation code. A maximum of 16 bytes (the whole register) can be read in a single read command. Figure 16 shows an example of a read command.

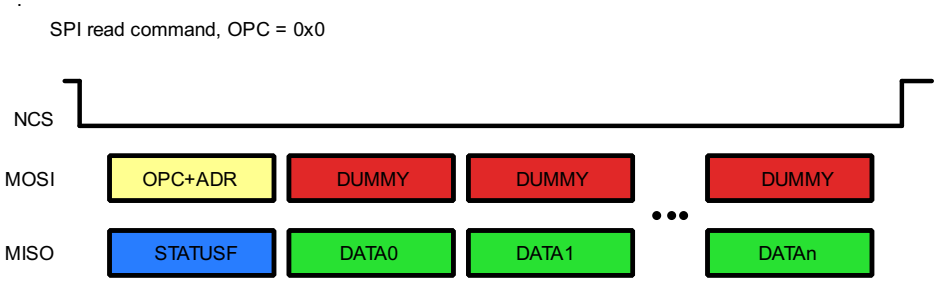


Figure 16: SPI read data

Write commands
Write commands can be divided into standard write and validable write.

A standard write command has the operation code 0xF and does not need a readout of the sent data to be validated. Nevertheless, in case of a non desired standard write (for example, due to communication noise), the command can be cancelled and data deprecated (not applied to iC-GFP configuration register). This can be achieved by sending more than 16 SPI frames (8 x SCLK pulses). In this case the configuration error flag COMOK will be cleared (cf. Figure 17). Once the desired number of data bytes is sent, the data can be validated by a rising edge at NCS.

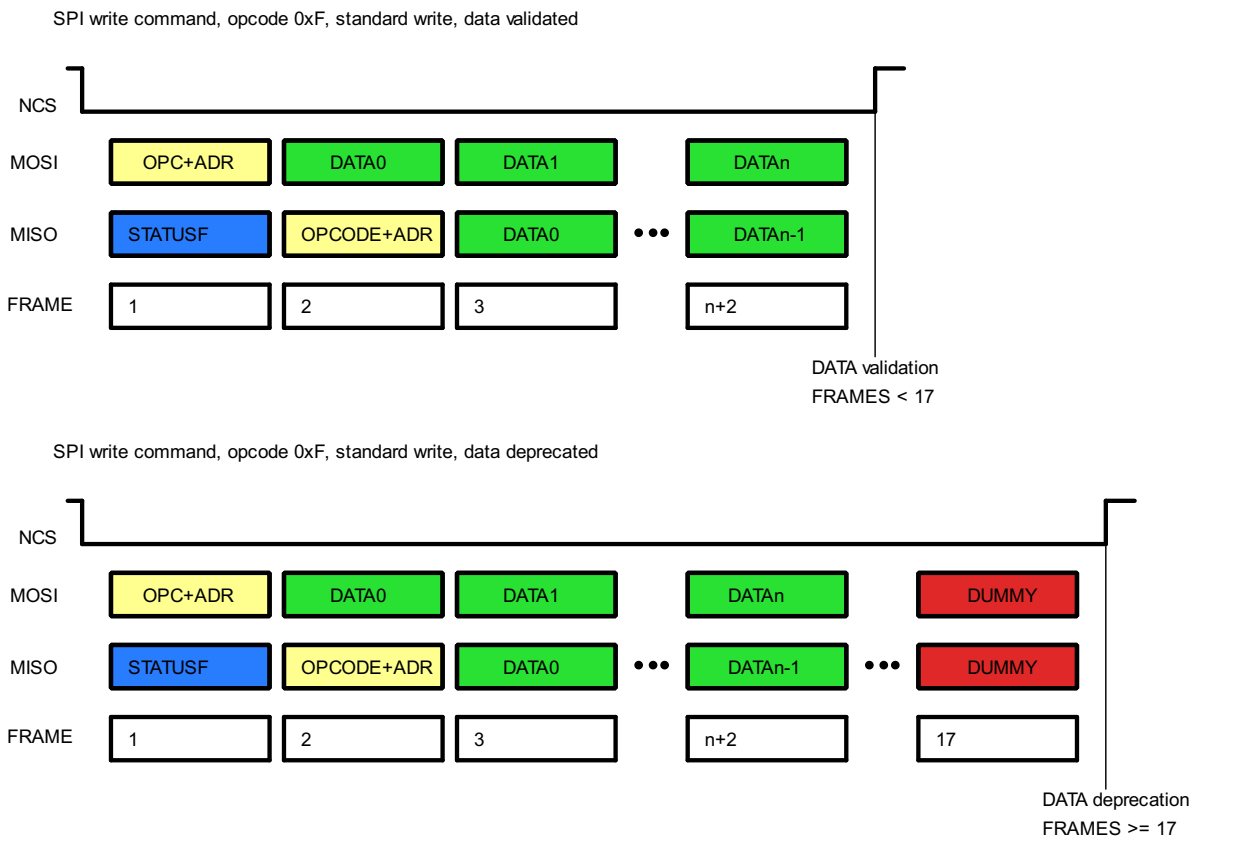


Figure 17: SPI standard write command

Write command with validation has an Opcode (OPC) from 0x1 to 0xE. The number of SPI frames must be the OPC + 2. This includes a dummy byte at the end of the command to readout and check the last byte. If the number of frames does not match, data will be deprecated and the configuration error flag COMOK will be cleared (cf. Figure 18). Once the defined number of data bytes is sent, the data can be validated by a rising edge at NCS. Validation applies to changed registers only. That means, if a register adress is loaded with a wrong value and not validated, this register can only be validated again after a new write access. In block access, after address 0x0F, both the address and the frame counter will not be increased (no loopback).

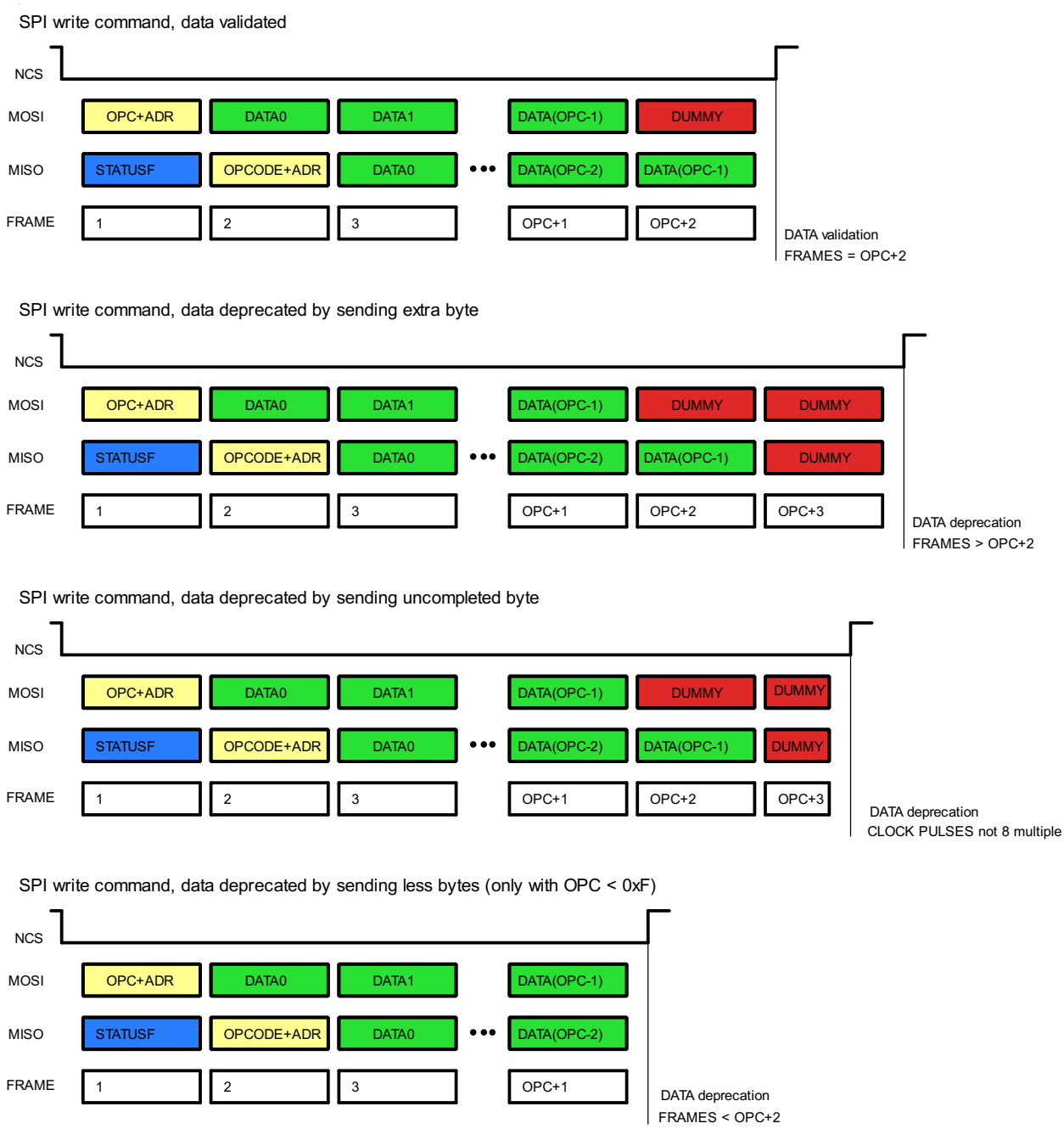


Figure 18: SPI write data

In adition to data validation, the SPI interface is protected against clock injection or suppression due to noise. At the rising edge of NCS (moment of data validation), the number of clock pulses received by the SPI interface must be a multiple of 8. Otherwise the data will not be validated and the configuration error flag, COMOK, will be cleared.

Procedure in case of faulty comunication

- During normal operation the content of the configuration RAM is applied directly to the chip and the MCU can read the configuration. Latches are transparent and act as buffers.
- When a communication error occurs (undesired clock injection or user commanded data deprecation), **all the latches** are disconnected from the RAM in order to preserve the last valid configuration. This is signaled by clearing COMOK.
- In this situation the MCU can only read back the contents of the RAM (possibly loaded with wrong data since an error occurred). The last valid configuration stored in the latches **is not readable** by the MCU and remains until a new valid write occurs.

- To ensure a correct recovery of the configuration RAM, it is mandatory to **rewrite every RAM register** with valid data. Following that, the latches are reconnected to the RAM and set transparent.
- After a communication error COMOK remains cleared untill **all the RAM registers from Adr. 0x01 to 0x0B** are newly written. In case of a partial re-write after a communication error, only the latches corresponding to the accessed registers will be reconnected to the RAM. The rest of the latches remains disconnected (storing the last valid configuration) until accessed again.

SPI timing definitions

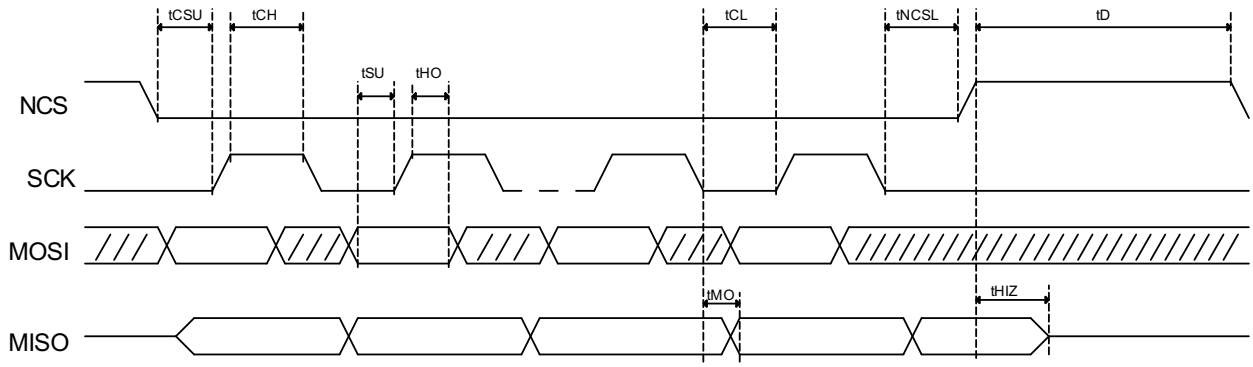


Figure 19: SPI timing

REGISTERS

Configuration overview

Table 74 shows an overview of the registers (read-only and status bits in blue).

OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0F	RAMOK	COMOK	VBOK	VCCOK	NVBREV	TEMPOK	NOVL2	NOVL1
0x00	SETV(1:0)		1	OENST	NCI2	NCI1	NTWRN	NWUD
0x01	IND2	IND1	OEXT2	OEN2	OUTD2	OEXT1	OEN1	OUTD1
0x02	SYNC	OPOL2	OCFG2(1:0)		WUS	OPOL1	OCFG1(1:0)	
0x03	HSP1	TEXC1	DTY1(1:0)		EXC1	OVLC1(2:0)		
0x04	HSP2	TEXC2	DTY2(1:0)		EXC2	OVLC2(2:0)		
0x05	PUNPD2	EPUCF2	CFPOL2	ENCF2	PUNPD1	EPUCF1	CFPOL1	ENCF1
0x06	SOVL	EVCC	O2FIL	IFOEN(1:0)		IFRX	IFTX(1:0)	
0x07	OENFIL(1:0)		CFIFIL(1:0)		CQFIL(1:0)		TXFIL(1:0)	
0x08	MNVBREV	MCOMOK	MUVD	MOVL	MCI2	MCI1	MNTWRN	MWUD
0x09	RNDDIS	VHDIS	VHV(5:0)					
0x0A	RESERVED (set to 0)			UVFIL	UVTH(3:0)			
0x0B	TSET(7:0)							
0x0C	TCUR(7:0)							
0x0D	Factory settings (read only)				RID(3:0)			
0x0E	Factory settings (read only)							

Table 74: Register layout

There are two kinds of status bits:

- **Resulting from a single event.** Status bit keeps its value untill the according register is read: **RAMOK, COMOK, NCI2, NCI1, NWUD**
- **Resulting from a current device state.** Status bit automatically follows the current state: **VBOK, VCCOK, NVBREV, TEMPOK, NOVL2, NOVL1, SETV(1:0), OENST, NTWRN**

The registers are summarized below.

RAMOK	Addr. 0x0F; bit 7	R
0	RAM memory initialized; CQ, Q2 forced to HIZ	
1	RAM memory not initialized since last read	

Table 75: RAMOK status bit

COMOK	Addr. 0x0F; bit 6	R
0	Communication error occured, not all latches are in transparent mode	
1	No communication error occured, all latches are in transparent mode	

Table 76: COMOK status bit

VBOK	Addr. 0x0F; bit 5	R
0	VBO voltage lower than selected threshold (UVTH)	
1	VBO voltage higher than selected threshold (UVTH)	

Table 77: VBOK status bit

VCCOK	Addr. 0x0F; bit 4	R
0	VCC voltage lower than threshold	
1	VCC voltage higher than threshold	

Table 78: VCCOK status bit

NVBREV	Addr. 0x0F; bit 3	R
0	VBO voltage lower than VBR	
1	VBO voltage higher or equal to VBR	

Table 79: NVBREV status bit

TEMPOK	Addr. 0x0F; bit 2	R
0	Die temperature above dangerous level, CQ, Q2 forced to HIZ	
1	Die temperature below dangerous level	

Table 80: TEMPOK status bit

NOVL1	Addr. 0x0F; bit 0	R
0	CQ channel forced to HIZ due to overload	
1	CQ channel not overloaded	

Table 81: NOVL1 status bit

NOVL2	Addr. 0x0F; bit 1	R
0	Q2 channel forced to HIZ due to overload	
1	Q2 channel not overloaded	

Table 82: NOVL2 Status bit

OENST	Addr. 0x00; bit 4	R
0	CQ, Q2 forced to HIZ due to chip status (VBOK, TEMPOK, RAMOK, power-up delay, overload)	
1	CQ, Q2 released for user control	

Table 83: OENST status bit

SETV(1:0)	Addr. 0x00; bit 7:6	R
00	VCC regulator configured to 3.3 V	
01	VCC regulator configured to 5 V	
10	VCC regulator configured to 1.8 V	
11	VCC regulator configured to 2.5 V	

Table 84: SETV status

NCI1	Addr. 0x00; bit 2	R
0	CQ changed its value at least once since last read	
1	CQ didn't change its value since last read	

Table 85: NCI1 status bit

NCI2	Addr. 0x00; bit 3	R
0	CFI changed its value at least once since last read	
1	CFI didn't change its value since last read	

Table 86: NCI2 status bit

NTWRN	Addr. 0x00; bit 1	R
0	Die temperature above alarm threshold (TSET)	
1	Die temperature below or equal to alarm threshold (TSET)	

Table 87: NTWRN Status bit

NWUD	Addr. 0x00; bit 0	R
0	At least one wake-up event occurred since last read	
1	No wake-up event occurred since last read	

Table 88: NWUD status bit

IND1	Addr. 0x01; bit 6	R
0	Signal at CQ is low	
1	Signal at CQ is high	

Table 89: CQ status

IND2	Addr. 0x01; bit 7	R
0	Input Signal at CFI is low	
1	Input Signal at CFI is high	

Table 90: CFI status

OEN1	Addr. 0x01; bit 1	R/W 0
0	Channel CQ forced to HIZ (depends on IFOEN)	
1	Channel CQ enabled (depends on IFOEN)	

Table 91: OEN1

OEN2	Addr. 0x01; bit 4	R/W 0
0	Channel Q2 forced to HIZ (depends on IFOEN)	
1	Channel Q2 enabled (depends on IFOEN)	

Table 92: OEN2

OEXT1	Addr. 0x01; bit 2	R/W 0
0	Channel CQ controlled by OUTD1 bit	
1	Channel CQ controlled by TX pin (depends on IFTX)	

Table 93: OEXT1

OEXT2	Addr. 0x01; bit 5	R/W 0
0	Channel Q2 controlled by OUTD2 bit	
1	Channel Q2 controlled by TX pin (depends on IFTX)	

Table 94: OEXT2

OUTD1	Addr. 0x01; bit 0	R/W 0
0	Channel CQ activated (controlled by OPOL1 and OCFG1)	
1	Channel CQ deactivated (controlled by OPOL1 and OCFG1)	

Table 95: OUTD1

OUTD2	Addr. 0x01; bit 3	R/W 0
0	Channel Q2 activated (controlled by OPOL1 and OCFG1)	
1	Channel Q2 deactivated (controlled by OPOL1 and OCFG1)	

Table 96: OUTD2

OCFG1	Addr. 0x02; bit (1:0)	R/W 11
00	CQ set to HIZ	
01	CQ configured as low-side driver	
10	CQ configured as high-side driver	
11	CQ configured as push-pull driver	

Table 97: CQ configuration

OCFG2	Addr. 0x02; bit (5:4)	R/W 11
00	Q2 set to HIZ	
01	Q2 configured as low-side driver	
10	Q2 configured as high-side driver	
11	Q2 configured as push-pull driver	

Table 98: Q2 configuration

HSP1	Addr. 0x03; bit 7	R/W 0
0	CQ set to normal speed mode	
1	CQ set to high speed mode	

Table 99: CQ High speed mode

HSP2	Addr. 0x04; bit 7	R/W 0
0	Q2 set to normal speed mode	
1	Q2 set to high speed mode	

Table 100: Q2 High speed mode

WUS	Addr. 0x02; bit 3	R/W 0
0	CQ is the source channel for wake-up	
1	CFI is the source channel for wake-up	

Table 101: Wake-up source channel

SYNC	Addr. 0x02; bit 7	R/W 0
0	Synchronized outputs disabled	
1	Synchronized outputs enabled (depends on OPOL2)	

Table 102: Synchronized outputs

OPOL1	Addr. 0x02; bit 2	R/W 0
0	CQ not inverted	
1	CQ inverted	

Table 103: CQ output polarity

OPOL2	Addr. 0x02; bit 6	R/W 0
0	Q2 not inverted	
1	Q2 inverted	

Table 104: Q2 output polarity

OVLC1(2:0)	Addr. 0x03; bit (2:0)	R/W 101
0x0	Min. current (cf. Electrical Characteristic No. 103)	
...		
0x5	200 mA ensured (cf. Electrical Characteristic No. 103)	
...		
0x7	Max. current	

Table 105: Short circuit current in CQ

OVLC2(2:0)	Addr. 0x04; bit (2:0)	R/W 101
0x0	Min. current (cf. Electrical Characteristic No. 203)	
...		
0x5	200 mA ensured (cf. Electrical Characteristic No. 203)	
...		
0x7	Max. current	

Table 106: Short circuit current in Q2

DTY1(1:0)	Addr. 0x03; bit (5:4)	R/W 10
00	Duty cycle of 1:4	
01	Duty cycle of 1:8	
10	Duty cycle of 1:10	
11	Duty cycle of 1:15	

Table 107: Overload detection duty cycle for CQ

DTY2(1:0)	Addr. 0x04; bit (5:4)	R/W 10
00	Duty cycle of 1:4	
01	Duty cycle of 1:8	
10	Duty cycle of 1:10	
11	Duty cycle of 1:15	

Table 108: Overload detection duty cycle for Q2

EXC1	Addr. 0x03; bit 3	R/W 0
0	CQ excitation current disabled	
1	CQ excitation current enabled	

Table 109: CQ excitation current selection

EXC2	Addr. 0x04; bit 3	R/W 0
0	Q2 excitation current disabled	
1	Q2 excitation current enabled	

Table 110: Q2 excitation current selection

TEXC1	Addr. 0x03; bit 6	R/W 0
0	CQ excitation current for typ. 2.5 µs	
1	CQ excitation current for typ. 7.5 µs	

Table 111: CQ excitation current duration

TEXC2	Addr. 0x04; bit 6	R/W 0
0	Q2 excitation current for typ. 2.5 µs	
1	Q2 excitation current for typ. 7.5 µs	

Table 112: Q2 excitation current duration

CFPOL1	Addr. 0x05; bit 1	R/W 0
0	CQ hi → RX1 hi	
1	CQ hi → RX1 lo	

Table 113: CQ input polarity

CFPOL2	Addr. 0x05; bit 5	R/W 0
0	CFI hi → RX2 hi	
1	CFI hi → RX2 lo	

Table 114: CFI input polarity

EPUCF1	Addr. 0x05; bit 2	R/W 1
0	CQ pull-up/down disabled	
1	CQ pull-up/down enabled	

Table 115: Enable pull-up/down CQ

EPUCF2	Addr. 0x05; bit 6	R/W 1
0	CFI pull-up/down disabled	
1	CFI pull-up/down enabled	

Table 116: Enable pull-up/down CFI

PUNPD1	Addr. 0x05; bit 3	R/W 0
0	Pull-down current	
1	Pull-up current	

Table 117: Current polarity at CQ

PUNPD2	Addr. 0x05; bit 7	R/W 0
0	Pull-down current	
1	Pull-up current	

Table 118: Current polarity at CFI

ENCF1	Addr. 0x05; bit 0	R/W 0
0	CQ feedback channel disabled	
1	CQ feedback channel enabled	

Table 119: CQ feeback channel enable

ENCF2	Addr. 0x05; bit 4	R/W 0
0	CFI feedback channel disabled	
1	CFI feedback channel enabled	

Table 120: CFI feeback channel enable

IFTX(1:0)	Addr. 0x06; bit (1:0)	R/W 10
00	CQ and Q2 controlled by TX1; TX2 has no effect	
01	CQ controlled by TX2; Q2 controlled by TX1	
10	CQ controlled by TX1; Q2 controlled by TX2	
11	CQ and Q2 controlled by TX2; TX1 has no effect	

Table 121: TX1, TX2 configuration

IFRX	Addr. 0x06; bit (2)	R/W 0
0	RX1 controlled by CQ; RX2 controlled by CFI	
1	RX1 controlled by CFI; RX2 controlled by CQ	

Table 122: RX1, RX2 pins configuration

IFOEN(1:0)	Addr. 0x06; bit (4:3)	R/W 11
00	OEN has no effect; CQ, Q2 controlled by corresponding OENx bit	
01	OEN controls only CQ; OEN1 bit has no effect	
10	OEN controls only Q2I; OEN2 bit has no effect	
11	OEN controls CQ and Q2; OEN1 and OEN2 bits have no effect	

Table 123: OEN pin configuration

SOVL	Addr. 0x06; bit 6	R/W 1
0	Normal overload detection mode	
1	Smart overload detection mode	

Table 124: Overload mode configuration

CQFIL(1:0)	Addr. 0x07; bit (3:2)	R/W 01
00	Filter disabled	
01	4 µs filter	
10	7 µs filter	
11	16 µs filter	

Table 125: CQ feedback channel filter configuration

CFIFIL(1:0)	Addr. 0x07; bit (5:4)	R/W 01
00	Filter disabled	
01	4 µs filter	
10	7 µs filter	
11	16 µs filter	

Table 126: CFI feedback channel filter configuration

OENFIL(1:0)	Addr. 0x07; bit (7:6)	R/W 10
00	Filter disabled	
01	3 µs filter	
10	8 µs filter	
11	15 µs filter	

Table 127: OEN pin filter configuration

EVCC	Addr. 0x06; bit (6)	R/W 1
0	VCC regulator disabled	
1	VCC regulator enabled	

Table 128: VCC regulator control

TXFIL(1:0)	Addr. 0x07; bit (1:0)	R/W 10
00	Filter disabled	
01	1 µs filter	
10	4 µs filter	
11	7 µs filter	

Table 129: TX1, TX2 filter configuration

O2FIL	Addr. 0x06; bit 5	R/W 1
0	Filter at TX2 disabled	
1	Filter at TX2 enabled and controlled by TXFIL	

Table 130: TX2 filter disable

MNVBREV	Addr. 0x08; bit 7	R/W 1
0	NVBREV will not be signaled at NDIAG	
1	NVBREV will be signaled at NDIAG	

Table 131: NVBREV signaling mask

MCOMOK	Addr. 0x08; bit 6	R/W 1
0	COMOK will not be signaled at NDIAG	
1	COMOK will be signaled at NDIAG	

Table 132: COMOK signaling mask

MUVD	Addr. 0x08; bit 5	R/W 1
0	VCCOK will not be signaled at NDIAG	
1	VCCOK will be signaled at NDIAG	

Table 133: VCC Undervoltage signaling mask

MOVL	Addr. 0x08; bit 4	R/W 1
0	NOVLx will not be signaled at NDIAG	
1	NOVLx will be signaled at NDIAG	

Table 134: Overload signaling mask

MCI2	Addr. 0x08; bit 3	R/W 0
0	CI2 event will not be signaled at NDIAG	
1	CI2 event will be signaled at NDIAG	

Table 135: CI2 signaling mask

MCI1	Addr. 0x08; bit 2	R/W 0
0	CI1 event will not be signaled at NDIAG	
1	CI1 event will be signaled at NDIAG	

Table 136: CI1 signaling mask

MNTWRN	Addr. 0x08; bit (1)	R/W 1
0	NTWRN will not be signaled at NDIAG	
1	NTWRN will be signaled at NDIAG	

Table 137: Overtemperature signaling mask

MWUD	Addr. 0x08; bit (0)	R/W 1
0	NWUD will not be signaled at NDIAG	
1	NWUD will be signaled at NDIAG	

Table 138: Wake-up signaling mask

VHV(5:0)	Addr. 0x09; bit (5:0)	R/W 001011
0x00	VH regulated to the min voltage	
...		
0x04	VH regulated to 5 V (cf. Electrical Characteristics No.905)	
...		
0x0B	VH regulated to 6.75 V (cf. Electrical Characteristics No.905)	
...		
0x18	VH regulated to 10 V (cf. Electrical Characteristics No.905)	
...		
0x2C	VH regulated to 15 V (cf. Electrical Characteristics No.905)	
...		
0x3F	Not supported	

Table 139: DC/DC converter output voltage

VHDIS	Addr. 0x09; bit (6)	R/W 0
0	DC/DC converter enabled	
1	DC/DC converter disabled	

Table 140: DC/DC converter disabling

RNDDIS	Addr. 0x09; bit (7)	R/W 0
0	DC/DC converter noise spreading enabled	
1	DC/DC converter noise spreading disabled	

Table 141: DC/DC converter noise spreading

UVTH(3:0)	Addr. 0x0A; bit (3:0)	R/W 0100
0x0	VBO undervoltage setpoint to 4.5 V	
0x1	VBO undervoltage setpoint to 6 V	
0x2	VBO undervoltage setpoint to 7 V	
0x3	VBO undervoltage setpoint to 8 V	
0x4	VBO undervoltage setpoint to 9 V	
0x5	VBO undervoltage setpoint to 10 V	
0x6	VBO undervoltage setpoint to 11 V	
0x7	VBO undervoltage setpoint to 12 V	
0x8	VBO undervoltage setpoint to 13 V	
0x9	VBO undervoltage setpoint to 14 V	
0xA	VBO undervoltage setpoint to 15 V	
0xB	VBO undervoltage setpoint to 16 V	
0xC	VBO undervoltage setpoint to 17 V	
0xD	VBO undervoltage setpoint to 18 V	
0xE	VBO undervoltage setpoint to 19 V	
0xF	VBO undervoltage setpoint to 20 V	

Table 142: VBO undervoltage configuration.

UVFIL	Addr. 0x0A; bit (4)	R/W 0
0	VBO undervoltage filter set to typ. 0.1 ms	
1	VBO undervoltage filter set to typ. 1 ms	

Table 143: VBO undervoltage filter configuration

TSET(7:0)	Addr. 0x0B; bit (7:0)	R/W 11111111
0x00	Alarm threshold set to TCUR = 0x00	
...		
0xFF	Alarm threshold set to TCUR = 0xFF	

Table 144: Overtemperature alarm threshold

TCUR(7:0)	Addr. 0x0C; bit (7:0)	R
0x00	-56 °C	
...		
0xFE	198 °C	
0xFF	Invalid measure	

Table 145: Temperature sensor reading

RID(3:0)	Addr. 0x0D; bit (3:0)	R
0x0	Initial version GFP0	
0x1	Initial version GFP1	
0x2	Initial version GFPZ	
0x3	Initial version GFPZ1	
0x4	Initial version GFPY	

Table 146: Chip revision mark

EVALUATION BOARD

iC-GFP comes with a evaluation board for test purposes. Figures 20 and 21 show both the schematic and the component side of the evaluation board.

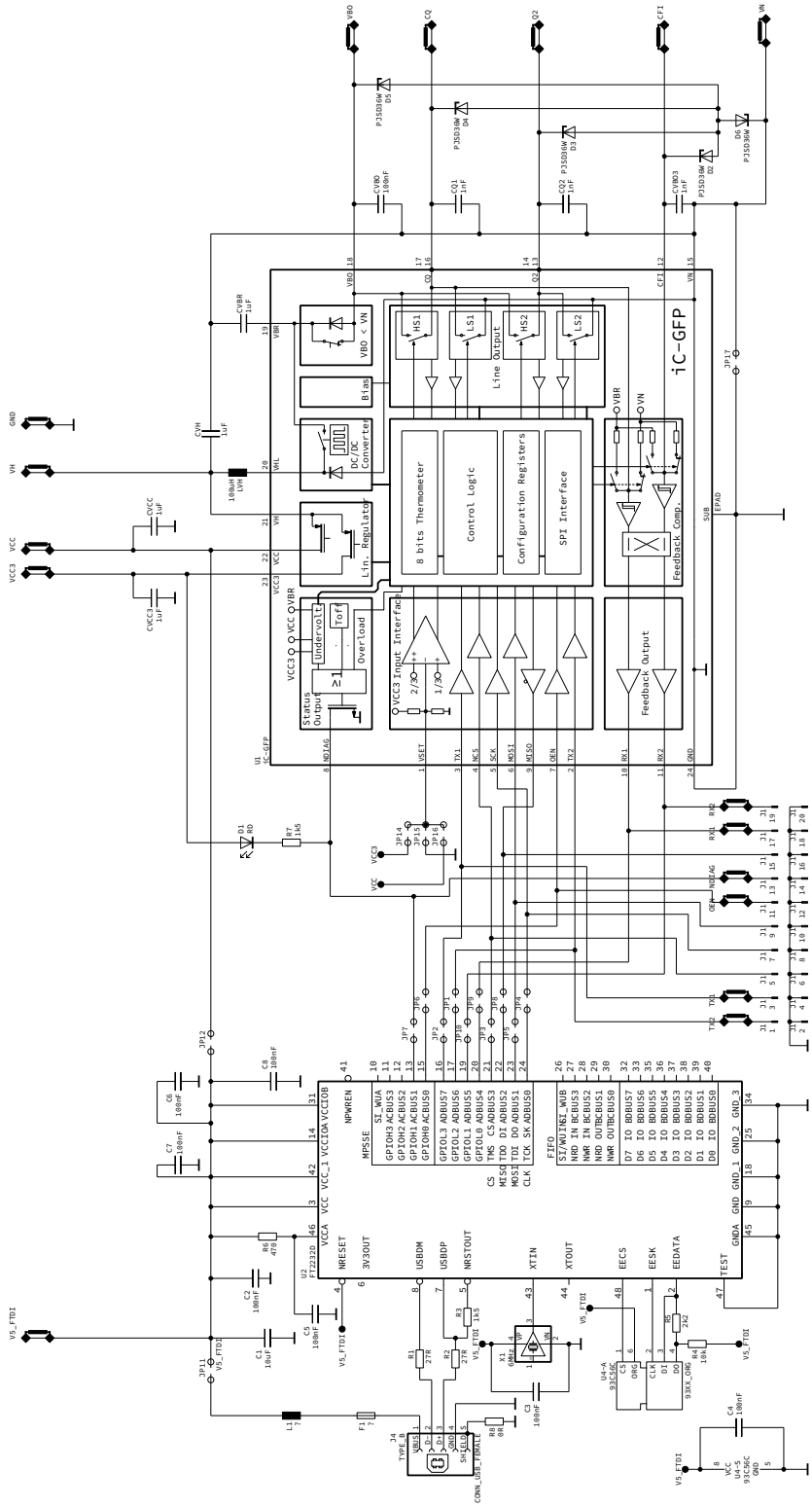


Figure 20: Schematic of the demo board

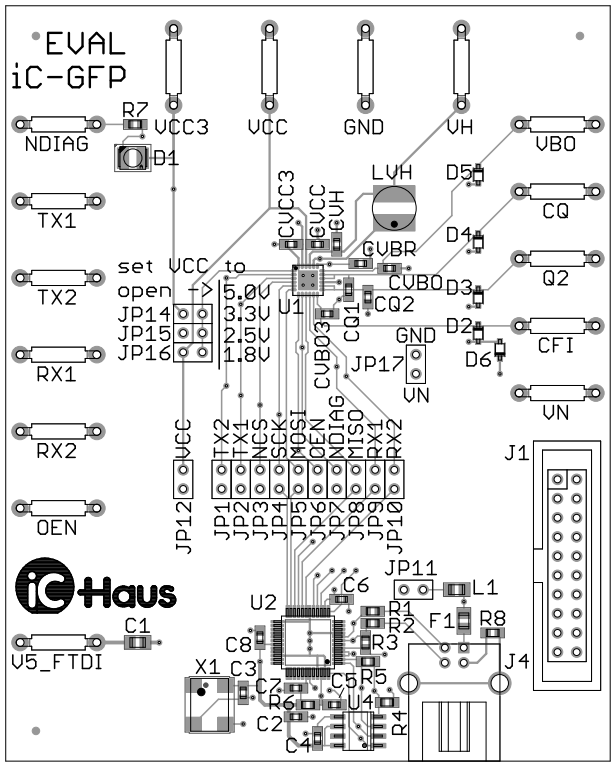


Figure 21: Demo board (component side)

DESIGN REVIEW / KNOWN ISSUES: Function Notes

iC-GFP Z		
No.	Function, parameter/code	Description and application notes
1	Overload detection, Electrical Characteristics Nos. 401/402	VBOK threshold shifted up 300 mV. Register bit UVTH Must be programmed to one position below to match datasheet.
2	Max. Load at VCC/VCC3, Operating Condition Item No. A01/B01, A03/B03	VCC and VCC3 regulators can be loaded up to 40 mA to ensure voltage limits in the whole temperature range

Table 147: Notes on chip functions regarding iC-GFP chip release Z (pre-serie)

iC-GFP Y		
No.	Function, parameter/code	Description and application notes
1	Chip revision RID(3:0)	Value updated to 0x4

Table 148: Notes on chip functions regarding iC-GFP chip release Y

REVISION HISTORY

Rel.	Rel. Date†	Chapter	Modification	Page
A1	2018-11-29		Initial Release	

† Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Order Designation
iC-GFP	QFN24 4 mm x 4 mm (RoHS compliant) Evaluation Board	iC-GFP QFN24-4x4 iC-GFP EVAL GFP1D

Please send your purchase orders to our order handling team:

Fax: +49 (0) 61 35 - 92 92 - 692
E-Mail: dispo@ichaus.com

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